**Abstract** — Inverted-staggered amorphous In–Ga–Zn–O (a-InGaZnO) thin-film transistors (TFTs) were fabricated and characterized on glass substrates. The a-InGaZnO TFTs exhibit adequate field-effect mobilities, sharp subthreshold slopes, and very low off-currents. The current temperature stress (CTS) on the a-InGaZnO TFTs was performed, and the effect of stress temperature (TSTR), stress current (ISTR), and TFT biasing condition on their electrical stability was investigated. Finally, SPICE modelling for a-InGaZnO TFTs was developed based on experimental data. Several active-matrix organic light-emitting-display (AMOLED) pixel circuits were simulated, and the potential advantages of using a-InGaZnO TFTs were discussed.

**Keywords** — Amorphous In–Ga–Zn–O (a-InGaZnO), thin-film transistor (TFT), current temperature stress (CTS), active-matrix organic light-emitting display (AMOLED).

**1 Introduction**

Active-matrix organic light-emitting displays (AMOLEDs) are now generally viewed as the next-generation display because of their vivid color, high contrast ratio, thin/light module, and low energy consumption.\(^1,2\) Although hydrogenated amorphous-silicon (a-Si:H) thin-film transistors (TFTs) currently dominate the liquid-crystal-display (LCD) market due to their uniformity over large area, low cost of fabrication, and mature technology, the insufficient field-effect mobility and metastable shift in threshold voltage when subjected to prolonged gate bias\(^3,4\) make their application to AMOLEDs rather difficult. [In AMOLEDs, the drive TFT has to constantly supply a current to the organic light-emitting diode (OLED) instead of just acting like a switch.] Larger devices and more-complex pixel circuits are needed to realize acceptable a-Si:H TFT AMOLEDs, which greatly limits the display resolution.\(^5,6\) As a result, TFTs based on other semiconductor materials have been explored as an alternative approach to realize reliable, high-resolution AMOLEDs.\(^7–9\)

Above all, amorphous In–Ga–Zn–O (a-InGaZnO) TFTs possess certain advantages including visible transparency, low processing temperature, good uniformity, adequate mobility, low off-current, sharp subthreshold swing, and potentially better electrical stability, which make them very attractive for AMOLEDs.\(^9–11\) Several a-InGaZnO TFT AMOLEDs have already been demonstrated by other groups, indicating a promising future for these devices.\(^12,13\) In this paper, we described properties of a-InGaZnO TFTs fabricated on glass substrates and studied their electrical stability by performing current temperature stress (CTS) measurements. The effect of stress temperature (TSTR), stress current (ISTR), and TFT-biasing conditions on the electrical properties of a-InGaZnO TFTs were investigated. Finally, an a-InGaZnO TFT SPICE model was developed, based on experimental data. We simulated several voltage- and current-programmed a-InGaZnO TFT AMOLED pixel circuits and analyzed their advantages over a-Si:H TFTs.

**2 TFT fabrication and characterization**

The a-InGaZnO TFTs were fabricated on glass substrates. The gate electrode Ti (5 nm)/Au (40 nm)/Ti (5 nm) was deposited by electron-beam deposition and patterned by lift-off. The gate insulator SiO\(_2\) (200 nm) and a-InGaZnO thin film were both deposited by RF sputtering and patterned by wet etching. After annealing in air at 300°C for 20 minutes, the source/drain electrodes Ti (5 nm)/Au (100 nm)/Ti (5 nm) were deposited by electron-beam deposition and patterned by lift-off. A SiO\(_2\) film as the back-channel protection layer (100 nm) was deposited by RF sputtering and patterned by wet etching. Finally, the TFTs were annealed in air at 200°C for 1 hour.\(^14\) Electrical measurements were performed in the dark using a Hewlett-Packard 4156A semiconductor parameter analyzer. The measured TFT transfer and output characteristics are shown in Fig. 1. The a-InGaZnO TFTs exhibit very low off-current, a sharp subthreshold swing (0.4 V/dec), a threshold voltage (V\(_T\)) of ~2 V, and field-effect mobility (\(\mu\)) of ~10 cm\(^2\)/V-sec. V\(_T\) and \(\mu\) were extracted by linearly fitting the I\(_D\)--V\(_{GS}\) curve to the standard MOSFET equation. The fitting range was chosen to be between 10% and 90% of the maximum measured I\(_D\) (V\(_{GS}\) = 20 V).\(^15\)
Current temperature stress (CTS) measurements were performed in the dark by using a Hewlett-Packard 4156A semiconductor parameter analyzer. The device temperature was regulated by a heated chuck and a Signatone temperature controller with a precision of 0.1 K. Before each measurement, the TFTs were placed on the heated chuck which is set at the desired measurement temperature for 30 minutes to allow for thermal equilibrium.

We used two different stress schemes for the CTS measurements: CTS\_lin and CTS\_sat.\(^{16,17}\) CTS\_lin and CTS\_sat are equivalent to operating the TFT in the linear and saturation regimes, respectively. For CTS\_lin, during the stress mode, the gate was biased at 20 V while a stress current ($I_{\text{STR}}$) was applied to the drain of the TFTs, as shown in Fig. 2(a). The same TFT were stressed for a total stress time ($t_{\text{STR}}$) of 10,000 sec, as illustrated in Fig. 3. At certain times ($t_{\text{STR}} = 100, 200, 500, 1000, 2000, 4000, 6000, 8000, \text{ and } 10,000 \text{ sec}$), the stress mode was interrupted and switched to the sweep mode where a quick gate voltage sweep ($V_{\text{GS}} = -5 \rightarrow 20 \text{ V}$) was applied to measure the transfer characteristic in the saturation regime of operation ($V_{\text{DS}} = 20 \text{ V}$). For CTS\_sat, during the stress mode, the gate and drain were externally shorted together, and $I_{\text{STR}}$ was applied to the drain, setting the voltages at the gate/drain ($V_{\text{GS}} = V_{\text{DS}}$), as shown in Fig. 2(b). The total stress time and number of points when the stress mode was interrupted are the same as CTS\_lin. In the sweep mode, the gate/drain voltages ($V_{\text{GS}} = V_{\text{DS}}$) were swept from $-5$ to 20 V to measure the transfer characteristics in the saturation regime. The same measurement procedure described above was repeated for several levels of stress current ($I_{\text{STR}}$) and stress temperature ($T_{\text{STR}}$) for both CTS setups. Table 1 summarizes the CTS conditions used in this study. For both CTS setups, after the 10,000 sec CTS measurement, the TFT was

### Table 1 — CTS conditions used in this study.

<table>
<thead>
<tr>
<th>Stress mode</th>
<th>Sweep mode</th>
<th>$I_{\text{STR}}$ (μA)</th>
<th>$T_{\text{STR}}$ (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTS_lin</td>
<td>$V_{\text{GS}} = 20 \text{ V}$, $V_{\text{DS}} = V_{\text{DS}}$</td>
<td>10, 40, 60, 70, 80</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{\text{GS}} = -5 \rightarrow 20 \text{ V}$, $V_{\text{DS}} = 20 \text{ V}$</td>
<td>1, 10, 40, 100</td>
<td></td>
</tr>
<tr>
<td>CTS_sat</td>
<td>$V_{\text{GS}} = V_{\text{DS}} = 20 \text{ V}$</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{\text{GS}} = -5 \rightarrow 20 \text{ V}$, $V_{\text{DS}} = V_{\text{DS}}$</td>
<td>40, 50, 60, 70, 80</td>
<td></td>
</tr>
</tbody>
</table>

* $V_{\text{GS}}$ increases with $\Delta V_T$ during the stress mode.
** $V_{\text{DS}} = V_{\text{GS}}$ increases with $\Delta V_T$ during the stress mode.
annealed at 300°C in air for 1 hour to recover its initial characteristics, as shown in Fig. 4.

3.2 CTS effect on a-InGaZnO TFT electrical properties

Figure 5(a) shows an example of the TFT transfer characteristics measured during the sweep mode \((V_{DS} = 20\, \text{V}, V_{GS} = -5 \rightarrow 20\, \text{V})\) of CTS_lin. The CTS_lin was performed at \(T_{\text{STR}} = 80^\circ\text{C}\) with \(V_{GS}\) held at 20 V, and \(I_{\text{STR}} = 10\, \mu\text{A}\). For this level of stress current \((I_{\text{STR}} = 10\, \mu\text{A})\), the drain-to-source voltage \((V_{DS})\) of the TFT is measured to be around 0.6 V, which indeed corresponds to the linear regime of operation. Figure 5(b) shows an example of the TFT transfer characteristics measured during the sweep mode \((V_{DS} = V_{GS} = -5 \rightarrow 20\, \text{V})\) of CTS_sat. The CTS_sat was performed at \(T_{\text{STR}} = 80^\circ\text{C}\) with the gate and drain tied together, and \(I_{\text{STR}} = 100\, \mu\text{A}\), which sets \(V_{GS} = V_{DS} \approx 16.5\, \text{V}\). As we can see from Fig. 5, even after suffering through these strict CTS conditions for \(10^4\) sec, the TFT subthreshold slope and off-current remained almost the same, the field-effect mobility slightly (10%) decreases, and the threshold voltage only shifted \(-2\, \text{V}\) for both CTS setups. Recently, it has been shown that the electrical stability of a-ZnSnO TFTs is highly dependent on the Zn/Sn ratio. 18 We believe it is possible that the electrical stability of a-InGaZnO TFTs can be further improved by optimizing the film chemical composition.

3.3 Stress-temperature (\(T_{\text{STR}}\)) effect

We performed CTS measurements for both CTS setups at stress temperatures ranging from 40°C to 80°C. The stress currents are 10 and 100 \(\mu\text{A}\) for CTS_lin and CTS_sat, respectively. \(I_{\text{STR}} = 10\, \mu\text{A}\) is sufficient for the maximum drive current level of a 15-in. XGA full-color AM-OLED (subpixel area \(A_{\text{pix}} \approx 30,000\, \mu\text{m}^2\)), assuming a brightness \((\nu)\) of 1000 cd/m² and an OLED efficiency \((\eta)\) of 5 cd/A:

\[
I_{\text{OLED}} = \frac{\nu \cdot A_{\text{pix}}}{\eta}.
\]  

We used a much higher \(I_{\text{STR}}\) for CTS_sat to enhance the TFT parameter shifts since we observed that the TFTs are electrically more stable when stressed under CTS_sat compared to CTS_lin for the same \(I_{\text{STR}}\) level (see the next section for further details). The device degradation is defined as the change in threshold voltage \((V_T)\):

\[
\Delta V_T = V_T(t = t_{\text{STR}}) - V_T(t = 0).
\]  

\(V_T\) was extracted from linearly fitting \(I_D^{1/2} - V_{GS}\) measured in the sweep mode. The fitting range is chosen to be \(V_{GS} = 5\rightarrow 20\, \text{V}\) to avoid the effect of the subthreshold regime at smaller \(V_{GS}\) values. It should be noted that the fitting range would affect the extracted \(V_T\), due to the non-linearity of the \(I_D^{1/2} - V_{GS}\) curve, and therefore should be carefully chosen.
Figures 6(a) and 6(b) show the TFT threshold voltage shift ($\Delta V_T$) as a function of stress time ($t_{STR}$) for various $T_{STR}$ under CTS_lin and CTS_sat, respectively. For both CTS setups, $\Delta V_T$ increases with $T_{STR}$ for a given $t_{STR}$. We also observed that

$$\Delta V_T \approx t_{STR}^\beta.$$  

$\beta$ is extracted to be $0.4 \pm 0.05$ for our a-InGaZnO TFTs. We have not observed any temperature dependence of $\beta$ in the investigated $T_{STR}$ range thus far.

A model that unifies the effect of stress temperature ($T_{STR}$) and stress time ($t_{STR}$) on defect creation was developed for a-Si:H TFTs. This model assumes a distribution of energy barriers $D(E_a)$ for defect creation exists during bias stress: after a time $t$ at a temperature $kT$ all possible defect-creation sites with $E_a \leq kT \ln(vt)$ will have converted into defects. The thermalization energy is therefore defined by

$$E = kT \ln(vt).$$

where $k$ is the Boltzmann constant and $v$ is the attempt-to-escape frequency. We investigated possible application of this thermalization energy concept to a-InGaZnO TFTs. By plotting $\Delta V_T$ as a function of $E$, a unique curve is obtained for both CTS setups with only one fitting parameter, the attempt to escape frequency $v$, as can be seen from Fig. 7. The value of $v$ is $10^7$ Hz for CTS_lin and $10^9$ Hz for CTS_sat and was determined to ensure the best overlap of the $\Delta V_T$–$E$ curves for all stress temperatures. It should be noticed that the thermalization energy is a function of $\ln(vt)$; therefore, the effect of $10^7$ and $10^9$ Hz are actually very close (14% difference). For a-Si:H TFTs, $v$ was extracted to be $10^{10}$ Hz and is believed to be associated with the breaking of weak Si–Si bonds. Although the physical meaning of $v$ is unclear for our a-InGaZnO TFTs, Eq. (4) describes very well our experimental data in the investigated $T_{STR}$ and $t_{STR}$ range.

### 3.4 Stress current ($I_{STR}$) effect

We also performed CTS measurements at various $I_{STR}$ levels. For CTS_lin, $I_{STR} = 1, 10, 40,$ and $100 \mu A$, and for CTS_sat, $I_{STR} = 40, 60, 80,$ and $100 \mu A$. Again, for CTS_sat, we did not explore lower $I_{STR}$ levels for the same reason mentioned previously. The stress temperature ($T_{STR}$) was fixed at 60°C. Figure 8 shows the threshold-voltage shift ($\Delta V_T$) as a function of $t_{STR}$ for various $I_{STR}$ levels under CTS_lin and CTS_sat. For CTS_lin, we can see that $\Delta V_T$ is almost independent of $I_{STR}$; on the other hand, for CTS_sat, $\Delta V_T$ increases with $I_{STR}$ and becomes independent of $I_{STR}$ once normalized to the injected charge $Q_{inj} = I_{STR} \times t_{STR}$, as shown in Fig. 9. $Q_{inj}$ is commonly used to evaluate the $\Delta V_T$ caused by trapped charge in the gate dielectric for c-Si MOSFETs. We attribute this behavior to the following. The $V_{GS}$ is fixed at 20 V for all levels of $I_{STR}$ in CTS_lin; therefore, the channel induced charge will remain almost the same as long as the TFT operates in the linear regime. However, in CTS_sat, the $V_{GS}$ adjusts accordingly to $I_{STR}$, and therefore, at higher $I_{STR}$ values, we have a higher $V_{GS}$, and thus more
channel-induced charge. The $V_{GS}$ and $V_{DS}$ values are summarized in Table 2 for both CTS setups and all $I_{STR}$ levels. We conclude from our experimental results that for the same $I_{STR}$, the a-InGaZnO TFTs are electrically more stable when $V_{GS}$ is smaller.

### 3.5 CTS measurement modeling

In CTS$_{sat}$, $V_{GS}$ increases with $V_T$ in order to maintain a constant $I_D$, which is similar to the $\Delta V_T$ compensation mechanism in AMOLED pixel circuits. A model that can describe/predict the $\Delta V_T$ as a function of stress time ($t_{STR}$), stress temperature ($T_{STR}$), and stress current ($I_{STR}$) is beneficial in designing AMOLED pixel circuits. A stretched-exponential model based on the charge injection/trapping concept was developed for a-Si:H TFTs when subject to constant voltage stress. We modified this model by taking into account that the gate overdrive voltage $[V_{GS}(t)-V_T(t)]$ is a constant during CTS$_{sat}$. An identical equation has also been derived for a-Si:H TFTs when subject to constant current stress, based on the carrier-induced defect creation model.4

$$\Delta V_T = \left[V_{GS}(t) - V_T(t)\right]^{\alpha} \left(\frac{t_{STR}}{\tau}\right)^{\beta},$$  \hspace{1cm} (5)

Equation (6) is not suitable for CTS$_{sat}$ or any current-programmed pixel circuits because we do not control $V_{GS}$ directly. It is, therefore, more straightforward to express Eq. (6) as a function of $I_{STR}$ by using

$$I_{STR} = \frac{1}{2+\gamma} \cdot K \cdot (V_{GS} - V_T)^{2+\gamma},$$ \hspace{1cm} (7)

where $K = (W/L)C_{ox} \mu_0$. By plugging Eq. (7) into Eq. (6), we can write the power-law equation as a function of $I_{STR}$ instead of gate overdrive voltage:

$$\Delta V_T = \left[\frac{2+\gamma \cdot I_{STR}}{K} \right]^{\alpha/(2+\gamma)} \left[1 + \frac{1}{2+\gamma}\right]^{\alpha} \left(\frac{t_{STR}}{\tau}\right)^{\beta}.$$ \hspace{1cm} (8)

The non-linear factor $\gamma$ was extracted to be $\sim 0.48$ for our a-InGaZnO TFTs. By plotting $\log(\Delta V_T)$ as a function of

<table>
<thead>
<tr>
<th>CTS condition</th>
<th>$I_{STR}$ (μA)</th>
<th>$V_{DS}$ (V)</th>
<th>$t_{STR} = 0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTS$_{lin}$</td>
<td>1</td>
<td>0.06</td>
<td></td>
</tr>
<tr>
<td>$V_{GS} = 20$</td>
<td>10</td>
<td>0.56</td>
<td></td>
</tr>
<tr>
<td>$T_{STR} = 60^\circ$</td>
<td>40</td>
<td>2.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>7.5</td>
<td></td>
</tr>
<tr>
<td>CTS$_{sat}$</td>
<td>40</td>
<td>11.9 (=$V_{GS}$)</td>
<td></td>
</tr>
<tr>
<td>$V_{GS} = V_{DS}$</td>
<td>60</td>
<td>13.8 (=$V_{GS}$)</td>
<td></td>
</tr>
<tr>
<td>$T_{STR} = 60^\circ$</td>
<td>80</td>
<td>15.5 (=$V_{GS}$)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>17.0 (=$V_{GS}$)</td>
<td></td>
</tr>
</tbody>
</table>

* During CTS$_{sat}$, $V_{DS}$ increases with $I_{STR}$. 

![FIGURE 8](image)

**FIGURE 8** — Threshold-voltage shift ($\Delta V_T$) as a function of stress time ($t_{STR}$) for various stress-current ($I_{STR}$) levels under (a) CTS$_{lin}$ and (b) CTS$_{sat}$.

![FIGURE 9](image)

**FIGURE 9** — Threshold-voltage shift ($\Delta V_T$) as a function of injected charge ($Q_{inj}$) for various stress-current ($I_{STR}$) levels under CTS$_{sat}$ (Ref. 17).
log(I_{STR}) for several levels of t_{STR}, as shown in Fig. 10, we can obtain $\alpha/(2 + \gamma) \sim 0.5$ from the slopes, and thus $\alpha \sim 1.24$.

On the other hand, CTS_lin can be modeled by the stretched-exponential model because $V_{GS}$ is held constant.

$$\Delta V_T = \left[ V_{GS} - V_{T0} \right]^{\alpha} \left[ 1 - \exp \left( - \frac{t_{STR}}{\tau} \right)^{\beta} \right].$$  \hspace{1cm} (9)

The simulation results of CTS_lin and CTS_sat are shown as the lines in Figs. 6 and 8. The same value of $\alpha = 1.24$ were used in both simulations. $\beta = 0.35$ for CTS_lin and $\beta = 0.44$ for CTS_sat. The fitting parameter $\tau$ as a function of $(kT_{STR})^{-1}$ is plotted in Fig. 11. $\tau_0$ is extracted to be 4.4 ms for both CTS setups, while $E_\tau = 0.7$ and 0.62 eV for CTS_lin and CTS_sat, respectively. The parameters used in CTS simulations are summarized in Table 3.

### 4 a-InGaZnO TFT AMOLED pixel-circuit simulation

#### 4.1 a-InGaZnO TFT for AMOLEDs

In the previous sections, we have explored the electrical properties and stability of a-InGaZnO TFTs and concluded that a-InGaZnO TFTs seem very promising for AMOLED application. The low off-current prevents the OLED current leaking from the TFTs during the off-state. The sharp subthreshold slope is beneficial to the TFT switching speed. The high field-effect mobility allows extra freedom when designing the pixel circuit. Smaller device sizes can be used, which increases the pixel aperture ratio. Moreover, lower gate overdrive voltages are sufficient to provide the desired current level. From the CTS measurement results obtained in this paper, lower gate overdrive voltages are also very beneficial to the TFT electrical stability. In the remaining sections of this paper, we will explore the possible application of a-InGaZnO TFTs to AMOLEDs by pixel-circuit simulations.

#### 4.2 a-InGaZnO TFT and OLED SPICE model

An a-InGaZnO TFT SPICE model was developed, based on the Rensselaer Polytechnic Institute (RPI) a-Si:H TFT model. The required a-InGaZnO TFT SPICE parameters were extracted from experimental data. A Synopsys HSPICE simulation tool was then used to simulate the TFT characteristics (illustrated as the open circles in Fig. 1). We can see that the RPI a-Si:H TFT model with appropriate a-InGaZnO TFT SPICE parameters can reproduce our measured device characteristics very well. To model the behavior of the OLED, we used two junction diodes $D_1$ $D_2$ (HSPICE diode model level (1)) with series resistors $R_{S1}$ and $R_{S2}$ connected in parallel with a capacitor $C$, shown in the inset of Fig. 12. SPICE parameters were extracted based on experimental data obtained within our group and summarized in Table 4.

### Table 3 — CTS modeling parameters.

<table>
<thead>
<tr>
<th></th>
<th>CTS_lin</th>
<th>CTS_sat</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\alpha$</td>
<td>1.24</td>
<td></td>
</tr>
<tr>
<td>$\beta$</td>
<td>0.35</td>
<td>0.44</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>NA</td>
<td>0.48</td>
</tr>
<tr>
<td>$\tau_0$</td>
<td>4.4 ms</td>
<td></td>
</tr>
<tr>
<td>$E_\tau$</td>
<td>0.7 eV</td>
<td>0.62 eV</td>
</tr>
</tbody>
</table>

### Table 4 — OLED SPICE parameters.

<table>
<thead>
<tr>
<th>Area</th>
<th>12000 $\mu$m$^2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>$I_S = 4.2$ nA, $n = 7.8$, $I_k = 13$ A</td>
</tr>
<tr>
<td>D2</td>
<td>$I_S = 60$ fA, $n = 3.6$, $I_k = 32$ mA</td>
</tr>
<tr>
<td>$R_{S1}$</td>
<td>2.6 m$\Omega$</td>
</tr>
<tr>
<td>$R_{S2}$</td>
<td>27 m$\Omega$</td>
</tr>
<tr>
<td>$C$</td>
<td>3 pF</td>
</tr>
</tbody>
</table>
rized in Table 4. The OLED area was assumed to be 12,000 µm² which is approximately the subpixel area of an RGB 3-in. QVGA display (63.5 × 190.5 µm). The OLED capacitor was calculated by assuming the capacitance per unit area is 25 nF/cm². The OLED I–V curve simulated by HSPICE is shown in Fig. 12.

4.3 Simple voltage-programmed pixel circuit

Thus far, all reported AMOLEDs driven by a-InGaZnO TFTs are based on the 2-TFT voltage-programmed pixel circuit,¹²,¹³ as shown in Fig. 13(a). Since this simple circuit does not compensate for the TFT threshold-voltage variation (∆V_T), the usage of this circuit requires the TFTs to be electrically very stable (∆V_T ~ 0). Synopsys HSPICE simulation tool with the a-InGaZnO TFT and OLED SPICE models developed in the previous section were used to evaluate the pixel-circuit performance. The simulated operation waveforms are shown in Fig. 14(a). Parameters used in the simulation are summarized in Table 5. Since the field-effect mobility of a-InGaZnO TFTs is ~10 times larger than that of a-Si:H TFTs, smaller device sizes (W/L = 24 µm/4 µm) and lower supply voltages (V_DD = 10 V) can be used in this circuit. We also investigated the effect of TFT threshold-voltage shift on the performance of this circuit, which will be discussed in later sections.

An additional TFT can be added to this circuit to prevent a sudden peak current from damaging the OLED, as shown in Fig. 13(b). The simulated operation waveforms are shown in Fig. 14(b). This circuit operates similar as the 2-TFT circuit except the current flows through the OLED only during the expose period.

4.4 Current-scaling current-mirror pixel circuit

The 2-TFT voltage-programmed pixel circuit is very simple in design and enables a high aperture ratio. However, due to the current-driven nature of OLEDs and their steep I–V characteristics, current-programmed pixel circuits are more suitable to precisely generate distinct gray levels. Moreover, even if the a-InGaZnO TFTs are electrically very stable, it is still desirable to use a pixel circuit that can compensate for any non-ideal factors. Several current-programmed pixel circuits were developed for AMOLEDs.²⁵–²⁷ Our group has previously explored the possible application of a-InGaZnO TFTs to a current-scaling pixel circuit that provides a wide dynamic OLED current (I_OLED) range and compensation abilities.²⁸ Here, we apply a-InGaZnO TFTs to a current-scaling current-mirror pixel circuit.²⁹ This circuit has similar performance as the previous circuit with a simpler driving scheme.

The current-scaling current-mirror pixel circuit consists of two switching TFTs (T1 and T2), one mirror TFT (T4), one driving TFT (T3), and two storage capacitors (C_ST1 and C_ST2) connected between the scan line and ground with a cascade structure, as shown in Fig. 15. The

![FIGURE 13 — Schematic diagrams of the (a) 2-TFT voltage-programmed pixel circuit and (b) the same circuit with an additional TFT (T3).](image)

![FIGURE 14 — Operation waveforms of the pixel circuits in Figs. 11(a), and 11(b), respectively, simulated by HSPICE.](image)

![FIGURE 12 — Simulated OLED I–V characteristics.](image)

![FIGURE 15 — Simulated OLED I–V characteristics.](image)

### TABLE 5 — Parameters used in HSPICE simulation for pixel circuits in Figs. 13(a) and 13(b).

<table>
<thead>
<tr>
<th></th>
<th>(a)</th>
<th>(b)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_DD (V)</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td>V_SCAN (V)</td>
<td>-1→10</td>
<td>-1→8</td>
</tr>
<tr>
<td>V_DATA (V)</td>
<td>NA</td>
<td>-1→8</td>
</tr>
<tr>
<td>C_ST (pF)</td>
<td>1</td>
<td>3→9</td>
</tr>
</tbody>
</table>
operation detail of this circuit can be found elsewhere. Parameters used to simulate this circuit are listed in Table 6 for both a-InGaZnO TFTs and a-Si:H TFTs. Smaller device sizes (W/ = 20 µm/4 µm) and lower supply voltages (VDD = 12 V) can be used for this circuit based on a-InGaZnO TFTs. Figure 15 shows an example of operation waveforms simulated by HSPICE.

4.5 Pixel-circuit simulation results

The OLED currents (I_OLED) delivered by the 2-TFT voltage-programmed pixel circuit and the 4-TFT current-scaling current-mirror pixel circuit as a function of V_DATA and I_DATA, respectively, are shown in Fig. 17. Since the OLED current value is different during the ON- and OFF-states (I_OLED_ON and I_OLED_OFF), we define the average OLED current (I_OLED) during one frame time as

\[
I_{OLED} = \frac{I_{OLED,ON} \cdot t_{ON} + I_{OLED,OFF} \cdot t_{OFF}}{t_{ON} + t_{OFF}},
\]

where t_ON (165 µsec) and t_OFF (16.5 msec) are the ON- and OFF-state periods, respectively (the frame rate is set to be 60 Hz). As we can see from Fig. 17, wide dynamic I_OLED range (~10^3) was achieved by both pixel circuits.

4.6 Impact of TFT instability on pixel-circuit operation

We also simulated the two pixel circuits assuming that the drive TFTs [T2 in Fig. 13(a), T3 and T4 in Fig. 15] exhibit 1 V of threshold-voltage shift (ΔV_T), as shown in Fig. 17. The percentage change in I_OLED (ΔI_OLED) is defined as

\[
\text{Percentage change in } I_{OLED} = \frac{I_{OLED} - I_{OLED,0}}{I_{OLED,0}} \times 100%.
\]
We can see that the 4-TFT current-scaling current-mirror pixel circuit can compensate for $\Delta V_T$ within operating error range from 9 to 25%, depending on the $I_{OLED}$ level, while the 2-TFT voltage-programmed pixel circuit does not compensate for $\Delta V_T$ at all ($\Delta I_{OLED}$: 40–90%). Keeping in mind that 1 V of $\Delta V_T$ is quite large compared to the small gate overdrive (0–5 V) designed to be used in the pixel-circuit simulations. To further investigate the compensation ability of the 4-TFT current-scaling current-mirror pixel circuit, we plotted $\Delta I_{OLED}$ as a function of $I_{OLED}$ for $\Delta V_T = 0.2$, 0.5, and 1 V, as shown in Fig. 18. We observe that $\Delta I_{OLED}$ is more severe at lower $I_{OLED}$ levels due to the smaller gate overdrive of the drive TFT. The percentage error can be maintained below 10% for all levels of $I_{OLED}$ if $\Delta V_T$ is smaller than 0.2 V. This result indicates that we need electrically very stable a-InGaZnO TFTs to be used for AMOLEDs.

5 Conclusion

We fabricated and characterized inverted-staggered a-InGaZnO TFTs on glass substrates. The TFTs exhibit adequate field-effect mobility, low off-current, and sharp subthreshold slope. To evaluate the electrical stability of a-InGaZnO TFTs, CTS measurements were performed. Several factors were considered, including the stress temperature, stress current, and biasing condition. We conclude that maintaining a lower temperature and smaller $V_{GS}$ is beneficial to the TFTs’ electrical stability, and for the same level of $I_D$, the TFTs are more stable when operating in the saturation regime then in the linear regime. The a-InGaZnO TFTs exhibit $\Delta V_T \sim 1$ V under 10,000 sec stress with $I_{STR} = 100$ µA, and $T_{STR} = 60°C$. The subthreshold slope, off-current, and field-effect mobility remain almost unchanged during the stress. Finally, a SPICE model was developed based on experimental data. Both simple voltage-programmed pixel circuits and current-programmed pixel circuits with $\Delta V_T$ compensation ability were simulated. Smaller device sizes and lower supply voltages could be used in a-InGaZnO TFT pixel circuits due to their superior electrical properties compared to those of a-Si:H TFTs. The voltage-programmed pixel circuits could be used provided that the a-InGaZnO TFTs are electrically very stable ($\Delta V_T \sim 0$ V). Otherwise, the current-programmed pixel circuit is needed to compensate for $\Delta V_T$. In conclusion, a-InGaZnO TFTs, if fully optimized, have great potential for higher resolution, lower power consumption, and more-stable operation AMOLEDs.

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References


