High Performance Silicon Nanowire Field Effect Transistors

Yi Cui,† Zhaohui Zhong,† Deli Wang,† Wayne U. Wang,† and Charles M. Lieber*†,‡
Department of Chemistry and Chemical Biology, and Division of Engineering and Applied Science, Harvard University, Cambridge, Massachusetts 02138

Received November 1, 2002

ABSTRACT

Silicon nanowires can be prepared with single-crystal structures, diameters as small as several nanometers and controllable hole and electron doping, and thus represent powerful building blocks for nanoelectronics devices such as field effect transistors. To explore the potential limits of silicon nanowire transistors, we have examined the influence of source-drain contact thermal annealing and surface passivation on key transistor properties. Thermal annealing and passivation of oxide defects using chemical modification were found to increase the average transconductance from 45 to 800 nS and average mobility from 30 to 560 cm2/V·s with peak values of 2000 nS and 1350 cm²/V·s, respectively. The comparison of these results and other key parameters with state-of-the-art planar silicon devices shows substantial advantages for silicon nanowires. The uses of nanowires as building blocks for future nanoelectronics are discussed.

Semiconductor nanowires (NWs)1−6 and carbon nanotubes (NTs)7−12 are attractive components for future nanoelectronics since they can exhibit a range of device function and at the same time serve as bridging wires that connect to larger scale metallization. For example, field effect transistors (FETs) have been configured from NWs1,3,4 and NTs7−11 by depositing the nanomaterial on an insulating substrate surface, making source and drain contacts to the NW or NT ends, and then configuring either a bottom or top gate electrode (Figure 1). This basic approach may serve as the basis for hybrid electronic systems consisting of nanoscale building blocks integrated with more complex planar silicon circuitry, although a number of issues including device performance, reproducibility, and integration will have to be addressed in order to realize such systems in the future.

In the case of NT FETs, considerable effort has been placed on improving key device parameters such as the carrier mobility and transconductance. For example, recent studies reported by Avouris and others9−12 have shown that the measured carrier mobility can be increased significantly by contact thermal annealing. The fact that NT samples consist of mixtures of semiconducting and metallic building blocks could, however, represent a hurdle to future developments in nanoelectronics.13 On the other hand, silicon nanowires (SiNWs) are always semiconducting, and the dopant type and concentration can be controlled during synthesis.1 SiNW building blocks may also be more readily integrated into silicon industry processing and fabrication than NTs,14 and thus might reduce barriers to the creation of hybrid structures.

Figure 1. (A) Schematic of a SiNW FET showing metal source and drain electrodes with the NW and contacts on the surface of SiO2/Si substrate. (inset) High-resolution transmission electron micrograph of a 5 nm diameter SiNW; the scale bar is 5 nm. (B) Scanning electron micrograph of a SiNW FET device; the scale bar is 500 nm.
Initial transport studies of SiNW FETs showed relatively low transconductance and carrier mobility ($\sim 0.01 \text{ cm}^2/\text{V s}$). Subsequent investigations of SiNW transistor characteristics in a crossed NW FET configuration indicated that the initial low transconductance and mobility values were due in part to poor contacts between the SiNWs and source-drain electrodes and are not intrinsic to the single-crystal NW building blocks (inset, Figure 1A). In this letter, we explore the limits of SiNW FETs by examining the influence of source-drain contact annealing and surface passivation on key transistor properties. Thermal annealing and passivation of oxide defects by chemical modification were found to increase the average transconductance from 45 to 800 nS and average mobility from 30 to 560 cm$^2$/V·s with peak values from 2000 nS and 1350 cm$^2$/V·s, respectively. Comparison of these results and other key parameters with state-of-the-art planar silicon devices shows substantial advantages for the SiNWs as building blocks.

The SiNWs used in these studies are boron-doped (p-type), 10–20 nm diameter single-crystal structures, prepared by a nanocluster-mediated growth method described previously. The SiNWs were deposited onto oxidized silicon substrates (600 nm thermal oxide) from ethanol suspension. Electrical contacts to the SiNWs were made by defining source-drain electrodes separated by 800–2000 nm with electron-beam lithography and subsequent evaporation of 50 nm Ti and 50 nm Au. Rapid thermal annealing was carried out at 300–600 °C for 3 min in the forming gas (10% H$_2$ in He) to improve the contact and passivate Si–SiO$_x$ interface traps. A typical SiNW device is shown in Figure 1B. Electrical transport measurements were performed in the air.

Source-drain contacts to SiNW FETs were made using Ti metal, and transport characteristics were studied as a function of annealing. In general, metal–silicon contacts have been well studied, and it is known that Ti can form a stable conducting silicide with a low Schottky barrier height on p-type silicon. Figure 2A shows the current (I) versus source-drain voltage ($V_{sd}$) behavior of a typical Ti-contacted SiNW device before and after thermal annealing. The I–$V_{sd}$ curves become more linear and symmetric, the conductance increases 3-fold, and the transport behavior becomes more stable after annealing. To characterize the reproducibility of these observations, we have made similar measurements on over 50 devices. These results are summarized in a histogram showing the frequency that different values of two-terminal resistance were observed (Figure 2B). Before annealing, the resistance shows a large distribution ranging from $\sim 100\text{ M}\Omega$ to $\sim 1\text{ G}\Omega$ with an average of 160 M$\Omega$. In contrast, the resistance after annealing has a narrower distribution of 0.1 to 10 M$\Omega$ with an average of 0.62 M$\Omega$; that is, a $260 \times$ improvement in the two-terminal conductance. The increased two-terminal conductance and stability can be attributed in part to better metal–SiNW contacts, although passivation of defects at Si–SiO$_x$ interface, which can occur during annealing, may also contribute to the observed enhancements.

We have also investigated how chemical passivation of the SiO$_x$ shell surrounding the single-crystal SiNW cores affects transport behavior (Figure 3A), since the Si/SiO$_x$/interface and SiO$_x$ surface defects could compensate the applied gate voltage and trap and scatter carriers. Surface modification was carried out by reaction with 4-nitrophenyl octadecanoate. This specific reagent was chosen since it will lead to a stable and relatively nonpolar Si–O–C ester linkage. Conductance ($I/V_{sd}$) versus backgate voltage ($V_g$) measurements were carried out before and after modification to assess clearly the effect of surface chemistry on characteristics of a specific SiNW FET.

In a typical device (Figure 3B), the conductance responds weakly to $V_g$ before modification. In contrast, the conductance is extremely sensitive to $V_g$ after modification and can be shut off at $V_g \sim 2.5$ V with an on/off ratio over 4 orders of magnitude. The transconductance after modification is an order of magnitude larger than before modification. Using a cylinder on an infinite plate model, we estimate a hole mobility of 1000 cm$^2$/V·s. This mobility is substantially larger than obtained in conventional Si devices. To assess the reproducibility of this surface chemistry and corresponding dramatic improvements in device behavior, we carried out experiments on a number of distinct SiNW devices. The summary of these results (Figure 3C and D) shows that transconductance and mobility increase an order of magnitude after modification. Significantly, the highest and the average hole mobility values of 1350 and 560 cm$^2$/V·s in p-SiNWs are more than an order of magnitude larger than the value for bulk Si, $\sim 40$ cm$^2$/V·s, at a comparable effective
insulator (SOI) structures being developed for future genera-
structurally and chemically analogous to the silicon-on-
creases in the transconductance and mobility (Figure 3E).

ammonium-modified NWs also show the significant in-
this idea, we have modified SiNW surfaces with tetraethyl-
observed improved transport behavior. Second, and to test
of polar surface sites, such as SiO
stability of the passivation, and moreover, that the passivation
accessibility of the surface to water hydrolysis may control
week and 1 day, respectively. These results suggest that
although the lifetime of the observed improvement was

First, the effect of chain length on characteristics of SiNW
passivation results, we have carried out other experiments.
To obtain additional information about the origin of these
passivation results, we have carried out other experiments.

average transconductance is ca. 10 times larger. These
improvements could lead to substantial benefits for high-
speed and high-gain devices. The SiNW FET devices also
improvements could lead to substantial benefits for high-
speed. Ignoring other factors, our mobility implies that
terahertz operation could be achieved in a ~2000 nm SiNW

For direct comparison of other key parameters, the SiNW
FET results have been scaled22 using the SOI FET gate length
of 50 nm and gate oxide thickness of 1.5 nm. Significantly,
the scaled on-state current (I_{on}) for the SiNW FET is larger
than state-of-the-art Si FETs, and moreover the average
subthreshold slope approaches the theoretical limit16 and the
average transconductance is ca. 10 times larger. These
improvements could lead to substantial benefits for high-
speed and high-gain devices. The SiNW FET devices also
have larger leakage currents, but this issue could be addressed
by implementing pn-diodes at the source and drain contacts
as in conventional MOSFETs. This comparison suggests that
efforts to make smaller SiNW FETs and explicitly test scaling
predictions could have an important impact in the future.

In conclusion, we have performed studies addressing the
origins of these FET performance with increases in the
mobility from 30 to 560 cm²/V s, average transconductance from 45 to 800 nS and average

doping concentration.16 The higher mobilities observed in
our SiNW devices may arise from improved structural
perfection and cylindrical morphology, although additional
studies are needed to address unambiguously this point. We
also note that these SiNW values are not upper bounds since
contacts and surface passivation have not been optimized.

Table 1. Comparison of the Key Device Parameters between Si Nanowire and SOI FET

<table>
<thead>
<tr>
<th></th>
<th>nanowire raw data</th>
<th>nanowire converted22</th>
<th>planar Si device21</th>
</tr>
</thead>
<tbody>
<tr>
<td>gate length (nm)</td>
<td>800–2000</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>gate oxide thickness (nm)</td>
<td>600</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>mobility (cm²/V s)</td>
<td>230–1350</td>
<td>230–1350</td>
<td>650</td>
</tr>
<tr>
<td>I_{on} (µA/µm)</td>
<td>50–200</td>
<td>2000–5600</td>
<td>650</td>
</tr>
<tr>
<td>I_{off} (nA/µm)</td>
<td>2–50</td>
<td>4–45</td>
<td>9</td>
</tr>
<tr>
<td>subthreshold slope (mV/decade)</td>
<td>174–609</td>
<td>60</td>
<td>70</td>
</tr>
<tr>
<td>transconductance (µS/µm)</td>
<td>17–100</td>
<td>2700–7500</td>
<td>650</td>
</tr>
</tbody>
</table>

In conclusion, we have performed studies addressing the
origins of these FET performance with increases in the
mobility from 30 to 560 cm²/V s, average transconductance from 45 to 800 nS and average

Figure 3. (A) Schematic illustrating surface defect passivation. (B) Conductance vs V_g measured on the same SiNW before and after 4-nitrophenyl octadecanoate modification. Histograms of SiNW transconductance (C) and mobility (D) before and after 4-nitrophenyl octadecanoate modification. (E) Histogram of SiNW mobility values after modification with tetraethylammonium bromide. In plots (B) to (E), the green (red) color designates before (after) surface modification.

To obtain additional information about the origin of these
passivation results, we have carried out other experiments.
First, the effect of chain length on characteristics of SiNW
FETs was investigated. Immediately after modification, 18-
carbon and 6-carbon chains gave similar transport results,
although the lifetime of the observed improvement was > 1
week and 1 day, respectively. These results suggest that
accessibility of the surface to water hydrolysis may control
stability of the passivation, and moreover, that the passivation
of polar surface sites, such as SiO−, is important to the
observed improved transport behavior. Second, and to test
this idea, we have modified SiNW surfaces with tetraethyl-
ammonium bromide solutions. Significantly, tetraethyl-
ammonium-modified NWs also show the significant in-
creases in the transconductance and mobility (Figure 3E).
In addition, it is worth noting that our SiNW FETs are
structurally and chemically analogous to the silicon-on-
insulator (SOI) structures being developed for future genera-

Acknowledgment. We thank H. Park and L. Lauhon for
helpful discussion. C.M.L. acknowledges the Defense Ad-
vanced Research Projects Agency for generous support of
this work.

References
(18) SiNW surfaces were cleaned in O$_2$ plasma (20 W, 60 s, 0.4 Torr O$_2$) followed by reaction in (a) the pyridine solution with 0.5 mg/mL (dimethylamino)pyridine (Aldrich) and 1 mg/mL 4-nitrophenyl octadecanoate (or 4-nitrophenyl hexanoate, Aldrich) for 6 h, or (b) 1 M tetraethylammonium bromide (Aldrich) aqueous solution for 30 min. The devices were then rinsed and dried with nitrogen gas.
(22) The measured SiNW FET values (column 2) were scaled to the dimensions of a state-of-the-art MOSFET (column 4) assuming the contact resistance is much smaller than the channel resistance and the resistance of channel is proportional to length, and calculating the capacitance based on the cylinder on infinite plate model$^1$ and the current per unit width using a NW diameter 20 nm. Calculations do not account for interface trap states, and thus it should be possible to increase the transconductance further.