David Blaauw
Associate Professor of Electrical Engineering and Computer Science
UNIVERSITY OF MICHIGAN
Role in the Center: Co-Investigator
Areas of Research: High-performance and low-power VLSI circuits, particularly addressing nano-meter design issues pertaining to power, performance and robustness. His focus is on ground breaking circuit design approaches, such as self adapting circuit techniques and energy efficient near-subthreshold operation, to enable low power / high performance designs with order of magnitude higher performance characteristics in the nano-meter era.

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A. PROFESSIONAL PREPARATION

Duke University	Physics, B.S, 1986
	Computer Science, B.S, 1986
University of Illinois, Urbana-Champaign	Electrical Engineering, M.S., 1988
University of Illinois, Urbana-Champaign	Computer Science, Ph.D., 1991

B. APPOINTMENTS

Associate Professor, EECS Department, University of Michigan	8/2001-present
Engineering Manager, Advanced Design Technology, Motoloral, Inc.	9/1994-8/2001
Staff Engineer, Semiconductor Systems Design Technology Group	9/1993-10/1994
Development Staff Member, IBM Corporation, Endicott, New York	9/1992 - 9/1993

C. SYNERGISTIC ACTIVITIES

Professor Blaauw was with the Engineering Accelerator Technology Division, IBM Corporation, Endicott, as a Development Staff Member, until August 1993. From 1993 until August 2001, he worked for Motorola, Inc., Austin, TX, where he was the Manager of the High Performance Design Technology group. Since August 2001, he has been on the faculty of the University of Michigan, Ann Arbor, as an Associate Professor. At the University of Michigan Professor Blaauw has supervised 22 graduate students, including 15 Ph.D student, and, since coming to the University of Michigan, has graduated three Ph.D. students.

His work has focused on VLSI design, with particular emphasis on circuit analysis and optimization problems for high-performance and low-power designs. Professor Blaauw has published many books and articles, including over 200 refereed journal and conference articles. He was the Associate Editor for the IEEE transactions on Computer-Aided Design. He was the Technical Program Chair and General Chair for the International Symposium on Low Power Electronics and Design in 1999 and 2000, respectively, and was the Technical Program Co-Chair and member of the Executive Committee the ACM/IEEE Design Automation Conference in 2000 and 2001.

Professor Blaauw has received many honors and awards, including the 2004 IEEE Micro Top Picks special issue on the most industry relevant and significant papers of the year in computer architecture, and the University of Michigan Henry Russel Award for ”Exceptional Scholarship and Conspicuous Ability as a Teacher,” in 2004 from the Regents of the University. His papers have won best-paper awards at a number of top conferences, including the IEEE Custom Integrated Circuits Conference in 2003, the ACM/IEEE International Symposium on Microarchitecture in 2003, the ACM/IEEE Asia-Pacific Design Automation Conference in 2003 and the ACM/IEEE Design Automation Conference in June of 2000. Prof Blaauw won the prestigious IBM Faculty Award from IBM Center for Advanced Studies in 2003, as well as the Motorola Innovation Award in 1997, and the Motorola High Impact Technology Award in1996.

Professor Blaauw has received numerous research grants from the NSF Engineering Research Center (ERC) for Wireless Integrated Micro Systems (WIMS), NSF Information Technology Research (ITR), MARCO/DARPA - Giga-Scale Research Center (GSRC), the Semiconductor Research Corporation (SRC) and a number of industries.

D. RELATED PUBLICATIONS

1. Shidhartha Das, David Roberts, Seokwoo Lee, Sanjay Pant, David Blaauw, Todd Austin, Krisztin Flautner, Trevor Mudge, ”A Self-Tuning DVS Processor using Delay-Error Detection and Correction,” IEEE Journal of Solid-State Circuits (JSSC), April 2006, invited paper
2. Scott Hanson, Dennis Sylvester, David Blaauw, ”A New Technique for Jointly Optimization Gate Sizing and Supply Voltage in Ultra-Low Energy Circuits,” ACM/IEEE International Symposium on Low- Power Electronics and Design (ISLPED), September 2006
3. Sarvesh Kulkarni, Dennis Sylvester and David Blaauw ”A Statistical Approach to Body Bias Clustering for Post-Silicon Tuning,” ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 2006
4. Bo Zhai, Leyla Nazhandali, Javin Olson, Anna Reeves, Michael Minuth, Ryan Helfand, Sanjay Pant, David Blaauw, Todd Austin, ”A 2.60pJ/Inst. Subthreshold Sensor Processor for Optimal Energy Efficiency,” IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2006
5. Sanjay Pant, David Blaauw, ”An Active Decoupling Capacitance Circuit for Inductive Noise Suppression in Power Supply Networks,” IEEE International Conference on Computer Design (ICCD), October 2006
6. Bo Zhai, David Blaauw, Dennis Sylvester, Krisztin Flautner, ”The Limit of Dynamic Voltage Scaling and Insomniac Dynamic Voltage Scaling,” IEEE Transactions on Very Large Scale Integration Systems (T-VLSI), November 2005, pg. 1239-1252
7. Bo Zhai, Scott Hanson, David Blaauw, Dennis Sylvester, ”Analysis and Mitigation of Variability in Subthreshold Design,” ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 2005
8. Shidartha Das, Sanjay Pant, David Roberts, Seokwoo Lee, David Blaauw, Todd Austin, Trevor Mudge, Krisztin Flautner, ”A Self-Tuning DVS Processor Using Delay-Error Detection and Correction,” IEEE Symposium on VLSI Circuits (VLSI-Symp), June 2005
9. Nam Sung Kim, Krisztin Flautner, David Blaauw, Trevor Mudge, ”Circuit and Microarchitectural Techniques Reducing Cache Leakage Power,” IEEE Transactions on Very Large Scale Integration Systems (T-VLSI), Vol. 12, No. 2, February 2004
10. Dongwoo Lee, David Blaauw, Dennis Sylvester, ”Gate Oxide Leakage Current Analysis and Reduction for VLSI Circuits,” IEEE Transactions on Very Large Scale Integration Systems (T-VLSI), Vol. 12, No. 2, February 2004

E. RELATED PATENTS

1. ”Memory System having Fast and Slow Data Reading Mechanisms,” Patent Number 7,072,229, issued on July 4, 2006
2. ”Data Processor Memory Circuit,” Patent Number 7,055,007, issued on May 30, 2006
3. ”Memory System Having Fast and Slow Data Reading Mechanisms,” Patent Number 6,944,067, issued on September 13, 2005
4. ”Actively-Shielded Signal Wires,” Patent Number 6,919619, issued on July 19, 2005
5. ”Method and Apparatus for Controlling Current Demand in an Integrated Circuit”, Patent Number 6,819,538, issued on November 16, 2004
6. ”Cross Coupling Delay Characterization for Integrated Circuits,” Patent Number 6,799,153, issued on September 28, 2004
7. ”Iterative, Noise-Sensitive Method of Routing Semiconductor Nets,” Patent Number 6,480,998, issued on November 12, 2002