

**Michael P. Flynn, Senior Member, IEEE, Guggenheim Fellow**

Associate Professor and WIMS ERC Wireless Thrust Leader,  
Department of Electrical Engineering and Computer Science  
UNIVERSITY OF MICHIGAN

**Role in the Center: Communication Team Leader, Co-Investigator**

**Areas of Research:** Analog/RF, data conversion

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**A. PROFESSIONAL PREPARATION**

**National University of Ireland (UCC)**

Electrical Engineering, B.E., 1988

**National University of Ireland (UCC)**

Electrical Engineering, M.Eng.Sc., 1990

**Carnegie Mellon University**

Electrical Engineering, Ph.D., 1995

**B. APPOINTMENTS**

**Thrust Leader, WIMS ERC-Wireless Sector**

9/2000-present

**Associate Professor, EECS Department, University of Michigan**

2006-present

**Assistant Professor, EECS Department, University of Michigan**

2001-2006

**Adjunct Professor (Part-time Lecturer), National University of Ireland (UCC)**

1997-2001

**Fellow/Technical Director, Parthus Technologies PLC, Cork, Ireland**

1997-2001

**Member of Technical Staff, Texas Instruments DSP R&D Laboratory**

1995-1997

**C. SYNERGISTIC ACTIVITIES**

Michael P. Flynn was born in Cork, Ireland. From 1998 to 1991, he was with the National Microelectronics Research Centre, Cork. He was with National Semiconductor in Santa Clara, CA, from 1993 to 1995. From 1995 to 1997 he was a Member of Technical Staff with Texas Instruments, DSP R&D lab, Dallas, TX. During the four year period from 1997 to 2001, he was with Parthus Technologies, Cork, where he held the positions of Technical Director and Fellow. During that time, he was also a part-time faculty member at the Department of Microelectronics, National University of Ireland (UCC), Cork. Dr. Flynn joined the University of Michigan in 2001. His technical interests are in data conversion, gigabit serial transceivers, and RF circuits.

Dr. Flynn received the 1992-93 IEEE Solid-State Circuits Pre-doctoral Fellowship. He received the NSF Early Career Award in 2004. In March 2006, he received the 2005-2006 Outstanding Achievement Award from the Department of Electrical Engineering and Computer Science at the University of Michigan. He was Associate Editor of the IEEE Transactions on Circuits and Systems II from 2002 to 2004. He is an Associate Editor of the IEEE Journal of Solid State Circuits (JSSC) and serves on the Technical Program Committees of the International Solid State Circuits Conference (ISSCC) and the Asia Solid State Circuits Conference (A-SSCC). He is a Senior Member of the IEEE, a member of Sigma Xi. He is Thrust Leader responsible for Wireless Interfaces at Michigan's Wireless Integrated Microsystems NSF Engineering Research Center.

#### **D. RELATED PUBLICATIONS**

1. S. Park, Y. Palaskas, A. Ravi, R. Bishop and M. Flynn, A 3.5 GS/s 5-b Flash ADC in 90 nm CMOS, Custom Integrated Circuits Conference (CICC), September 2006.
2. S. Park and M. P. Flynn, A Regenerative Comparator Structure with Integrated Inductors, IEEE Transactions on Circuits and Systems I, vol. 53 no. 8, pp. 1704-1711, August 2006.
3. F. Kocer and M. P. Flynn, An RF Powered, Wireless CMOS Temperature Sensor, IEEE Sensors Journal, vol. 6, no. 3, June 2006, pp. 557-64, June 2006.
4. F. Kocer and M. P. Flynn, A New Transponder Architecture with On-Chip ADC for Long-Range Telemetry Applications, IEEE Journal of Solid-State Circuits, vol. 41, no. 5, pp. 1142-1148, May 2006.
5. S. Park, Y. Palaskas and M. P. Flynn, A 4GS/s 4bit Flash ADC in 0.18 $\mu$ m CMOS, IEEE International Solid State Circuits Conference (ISSCC), February 2006.
6. J. Chen, M. P. Flynn, and J. Hayes, A Fully Integrated Auto-Calibrated Super-Regenerative Receiver, IEEE International Solid State Circuits Conference (ISSCC), February 2006.
7. M. P. Flynn and J. Kang, Global Signaling over Lossy Transmission Lines, in International Conference on Computer Aided Design (ICCAD), November 2005, Invited Tutorial Paper.
8. J. Kang, J. Park and M. P. Flynn, Global High-Speed Signaling in Nanometer CMOS, Asia Solid State Circuits Conference (ASSCC), November 2005.
9. J. Chen, M. P. Flynn and J. Hayes, A 3.6mW 2.4-GHz Multi-Channel Super-Regenerative Receiver in 130nm CMOS, Custom Integrated Circuits Conference (CICC), September 2005.
10. F. Kocer and M. P. Flynn, A Long-Range RFID IC with On-chip ADC in 0.25  $\mu$ m CMOS, IEEE Radio Frequency Integrated Circuits Conference (RFIC 2005). **\*\*Third Best Student Paper Award\*\***
11. J. Park and M. P. Flynn, Capacitively Averaged Multi-Phase LC Oscillators, International Conference on Circuits and Systems (ISCAS) 2005.
12. M. P. Flynn, S. Park, and C. C. Lee, Achieving Analog Accuracy in nanometer CMOS, International Journal of High Speed Electronics and Systems, vol. 5, no. 2, pp. 255-275, 2005.
13. F. Kocer and M. P. Flynn, Wireless, remotely powered telemetry in 0.25 $\mu$ m CMOS, IEEE Radio Frequency Integrated Circuits Conference (RFIC 2004), June 2004, pp. 339-342. **\*\*Second Best Student Paper Award\*\***
14. F. Kocer and M. P. Flynn, An Injection Locked, RF Powered, Telemetry IC in 0.25 $\mu$ m CMOS, 2004 VLSI Symposium, June 2004.
15. F. Kocer and M. P. Flynn, An RF powered, wireless temperature sensor in 0.25 $\mu$ m CMOS, International Symposium on Circuits and Systems, May 2004.
16. M. P. Flynn and I. Bogue, Using redundancy to break the link between accuracy and speed in an ADC, Instrumentation and Measurement Technology Conference (IMTC '03), Proceedings of the 20th IEEE, Vol: 1, pp. 850-853, May 10-22, 2003.
17. M. P. Flynn, C. Donovan, and L. Sattler, Digital Calibration Incorporating Redundancy of Flash ADCs, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 50, no. 5, pp. 205-214, May 2003.
18. C. Donovan and M. P. Flynn, A Digital 6-bit ADC in 0.25 $\mu$ m CMOS, IEEE Journal of Solid- State Circuits, pp. 432-437, March 2002.
19. D. J. Foley and M. P. Flynn, A Low-power 8-PAM Serial Transceiver in 0.5 $\mu$ m digital CMOS, IEEE Journal of Solid-State Circuit, pp. 310-316, March 2002.