Dennis Sylvester	1301 Beal Ave.
Associate Professor of Electrical Engineering and Computer Science	Room 2417D
UNIVERSITY OF MICHIGAN	Ann Arbor, MI, 48109-2122
Role in the Center: Processing Team Leader, Co-Investigator	Phone: (734) 615-8783
Areas of Research: My research focuses on pressing issues in high-	Fax: (734) 763-9324
performance VLSI circuit design and electronic design automation	E-mail: dennis@eecs.umich.edu
(EDA) in light of the aggressively scaled process geometries in mod-	
ern MOS technologies. My specific research interests are threefold:	

A. PROFESSIONAL PREPARATION

1) Low-power design and EDA; 2) Variability-aware design methodologies (i.e., Design for robustness); and 3) Interconnect modeling

University of Michigan	Electrical Engineering, B.S., 1995
University of California, Berkeley	Electrical Engineering, M.S., 1997
University of California. Berkelev	Electrical Engineering, Ph.D., 1999

B. APPOINTMENTS

and analysis.

Associate Professor, EECS Dept., University of Michigan	2005-present
Assistant Professor, EECS Dept., University of Michigan	2000-2005
Senior R&D Engineer, Synopsys, Inc., Advanced Technology Group	1999-2000

C. SYNERGISTIC ACTIVITIES

Professor Sylvester's research focuses on pressing issues in high-performance VLSI circuit design and electronic design automation (EDA) in light of the aggressively scaled process geometries in modern MOS technologies. My specific research interests are: 1) Low-power design and EDA; 2) Variability-aware design methodologies (i.e., Design for robustness); 3) Interconnect modeling and analysis; 4) Transistor- and gate-level low-power design techniques; 5) Design for manufacturability; 6) Compact on-chip interconnect modeling for timing and signal integrity; and 7) Design automation for post-CMOS nanoscale electronics. Over the past 5 years, he has graduated 3 Ph.D. students with many more on the way.

He has served as the Principal Investigator on many projects sponsored by SRC, NSF, DARPA, MARCO, INTEL, SUN, and other industries. He has published many book chapters and more than 40 papers in refereed journals. He has also had more than 100 papers and invited presentations in many national and international conferences and symposia. Professor Sylvester is a Senior Member of IEEE, and past General Chair of the ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems. He is also an Associate Editor for the IEEE Transactions on VLSI Systems.

Dr. Sylvester has received many awards including the Henry Russel Award from the Regents of The University of Michigan. He was also a recipient of a 2004 College of Engineering Outstanding Teaching Award, the 2003 ACM Outstanding New Faculty award, and the NSF CAREER award.

D. RELATED PUBLICATIONS

- 1. A. Srivastava, D. Sylvester, and D. Blaauw, *Statistical Analysis and Optimization for VLSI: Timing and Power*, Springer Publishers, New York, 2005.
- L. Stok, R. Puri, S. Bhattacharya, J. Cohn, D. Sylvester, A. Srivastava, and S.H. Kulkarni, "Pushing ASIC performance in a power envelope," in: *Closing the Power Gap Between ASIC and Custom*, D. Chinnery and K. Keutzer, ed., Springer Publishers, New York, 2005. (forthcoming)
- 3. S.H. Kulkarni, A. Srivastava, and D. Sylvester, "Power optimization techniques using multiple supply voltages," in: *Closing the Power Gap Between ASIC and Custom*, D. Chinnery and K. Keutzer, ed.,