InP-based material for optoelectronic integration and solar energy conversion

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ABSTRACT

The purpose of this thesis is to utilize InP-based materials to both process the lightwave signals with large scale photonic integrated circuits and harvest the solar power with cheap, high-efficiency thin-film type solar cells. In the first part of the thesis, the reconfigurable add-drop multiplexer (ROADM) is used as the demonstration target. Past ROADM technologies were limited to passive optical components. Here, we adopt an asymmetric twin waveguide (ATG) technology with multiple tapers to successfully couple the light between on-chip optical amplifier and on-chip p-i-n detector. Passive components such as optical switches, waveguides, and multiplexer/de-multiplexer are also successfully demonstrated with same InP material system. Finally, a ROADM circuit capable of performing channel add/drop was fabricated and characterized by monolithically integrating these individual optical components on-to the same InP substrate.

The second part of the thesis work focuses on realizing high-efficiency, thin-film InP-based solar cells. First, the motivation for developing III-V thin-film solar cells is illustrated via a cost analysis. Multiple choices of fabrication processes of InP thin-film solar cell, such as direct epitaxy, cold-welding with substrate removal, and cold-welding with epitaxial lift-off (ELO) are then demonstrated. For the process of cold-welding with ELO, the solar cell performance is compatible to that of a bulk counterpart. This process enables the preservation of the original InP substrate for regrowth following the thin-film solar cell fabrication.

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Introduction

Indium phosphide (InP) is a III-V compound semiconductor with zinc-blende crystal structure, direct-bandgap of 1.35 eV [1] and lattice constant of 5.86 Å [2] at room temperature. It is widely used as the substrate for optoelectronic devices due to its compatibility with quaternary InGaAsP alloys. Figure 1 shows the relationship of the bandgap to the lattice constant of $In_{1-x}Ga_xAs_yP_{1-y}$ [1] with the dotted line representing the alloys lattice-matched to InP. By carefully adjusting the composition of InGaAsP, the available bandgap lies within 0.75eV – 1.35eV which makes InP-based material system a popular choice for realizing light generation/detection devices operating within the wavelength range of 1.3 µm-1.55 µm. Knowledge of the energy band offset between the selective InGaAsP alloys is needed to determine the proper band-gap and dimension for the quantum structure to emit/detect light. In general, the conduction band offset for heterojunction of InGaAsP/InP is about 40% of their bandgap difference ΔE_g, while that of the AlGaAs/GaAs system accounts for 67% of ΔE_g [3]. On the other hand, higher bandgap, lattice-matched InGaAsP alloys can also be applied to make passive optoelectronic devices to guide the light operating at wavelengths of 1.3 µm or 1.55 µm. Table 1 [4] lists the refractive indices of commonly used lattice-matched InGaAsP alloys based on the model and experimental data described in Refs [5-6]. With these parameters, passive optoelectronic devices such as waveguides, optical switches, and multiplexers/de-multiplexers can be designed and fabricated. Hence, it is apparent that the InP-based material system provides a large degree of freedom to simultaneously realize active and passive optoelectronic devices.

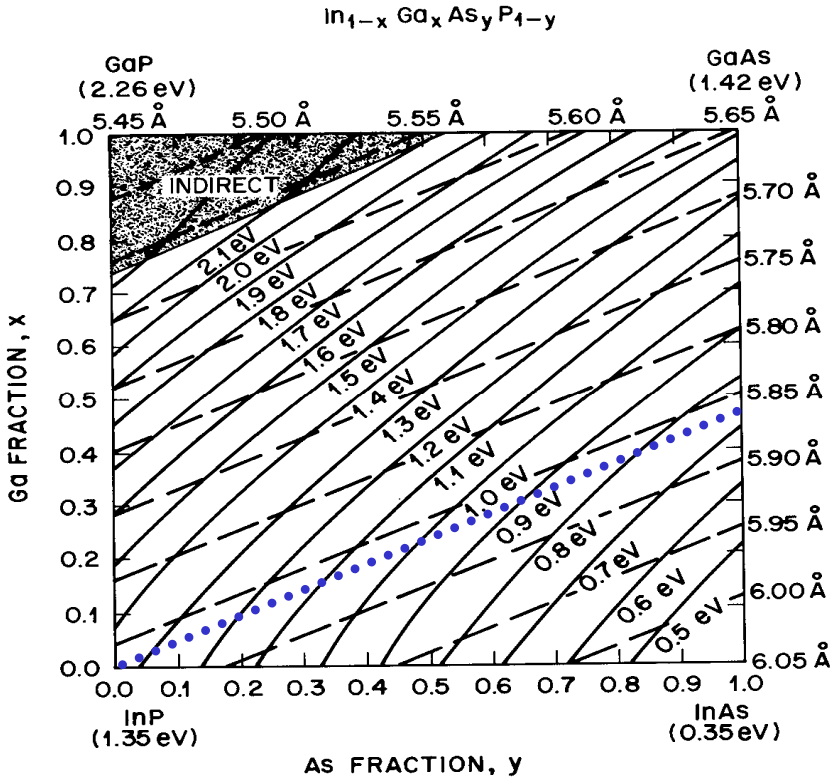

Figure 1 *Bandgap and lattice constant of $In_{1-x}Ga_xAs_yP_{1-y}$ [1]*

Material	λ_g	Index
$In_{0.81}Ga_{0.19}As_{0.43}P_{0.57}$	1.20 µm	3.3189
$In_{0.90}Ga_{0.10}As_{0.21}P_{0.79}$	1.05 µm	3.2405
$In_{0.80}Ga_{0.20}As_{0.70}P_{0.30}$	1.55 µm	3.6
InP	0.92 µm	3.1694

Table 1 *Composition, bandgap, and refractive index of commonly used InGaAsP quaternary alloys [4]*

The direct-bandgap of InP and its lattice-matched InGaAsP families also make them a good candidate for harvesting power from solar irradiation. The flexibility of tuning the bandgap of InGaAsP alloys especially provides a great chance to boost the efficiency of solar cells up to their thermodynamic limit. It has been modeled and demonstrated that concentrated solar cells consisting of $In_{0.89}Ga_{0.11}As_{0.25}P_{0.75}$ homojunction with bandgap of 1.14 eV exhibit power efficiency of 27.5% under 171 suns [7]. On the other hand, single-crystalline InP is useful in space-borne applications due to its high radiation hardness [8], compared to other III-V compounds. Currently, InP p-i-n homojunction solar cells with power efficiency of 22% under 1 sun [9] and InP/$In_{0.53}Ga_{0.47}As$ three-terminal tandem solar cells with power efficiency 31.8% [10] under 50 suns have been demonstrated. Surface Fermi level pinning also allows InP be useful in high-efficiency Schottky type solar cells by adopting ITO as the top contact [11]. The advantage of such Schottky type solar cells is their ease of fabrication, which avoids epitaxial growth, only requiring the process steps of sputtering and evaporation to define the electrodes. The challenge of InP-based solar cells is the lack of high-bandgap, lattice matched III-V alloys to serve as window layers to block the photo-generated carriers from diffusing towards the wrong electrodes. This issue has been currently mitigated by adopting heavily doped InP layer to create barriers height [9]. Nevertheless, this induced barrier is not high enough to sufficiently block the wrong-diffused photo-generated carriers and isolate them from the influence of the front surface recombination.

Dissertation outline

This dissertation is divided into two parts. The first part describes the functionality of InP-based monolithically integrated reconfigurable optical add-drop multiplexers (ROADM). ROADM is basically a photonic circuit which can upload and download any selected wavelength channels based on real-time internet traffic. This sophisticated circuit is required to simultaneously route multiple lightwave signals while providing high speed of light detection and high gain of light amplification. The material properties of InP and its InGaAsP alloys can potentially realize such a complicated functionality with the scheme of photonic integration. In Chap 1, we discuss the architecture of ROADM, including its various building block components and the data flow path during the operation of insertion (add) or download (drop) of a selected wavelength channel. Also, the photonic integration technology used in this work, asymmetric twin waveguide technology (ATG) [4], is introduced. Chapter 2 includes a discussion of the design, fabrication, and characterization, including the optical loss, crosstalk and wavelength sensitivity, of the passive components in the ROADM circuit – including an arrayed waveguide grating (AWG) and 2x2 optical switches. The detailed scheme for utilizing the same multiple quantum well (MQW) epi-layer for both providing the functionality of light amplification and detection in the ROADM is described in chapter 3.Finally, the implementation of the ROADM circuit by integrating all of the passive and active components in chapters 2 and 3 to an InP substrate will be described in chapter 4. Finally, in chapter 5, we go beyond the photonic domain by demonstrating an InP-based enhancement mode MOSFETs which could enable the integration of high speed electronics with complex photonic integrated circuits.

In second part of this thesis work, we demonstrate the feasibility of thin-film type III-V solar cells for solar power harvesting. An ITO/InP Schottky-type diode is chosen for its simplicity of device fabrication. In Chapter 6, we review the general principles and characterization techniques of solar cells. Then, the production costs of bulk and thin-film type solar cells are evaluated and compared. From Chap 7 to Chap 9, we demonstrate various ways to realize III-V thin-film solar cell with either material growth or direct bonding. Chap 7 describes MBE growth III-V thin-films on a quartz substrate. Chapter 8 discusses the fabrication and the characteristics of ITO/InP thin-film solar cells cold-welded onto Kapton substrates. To further reduce the fabrication cost, it is necessary to re-use the original III-V seed substrate for material re-growth after each round of the fabrication of the III-V thin-film solar cell. Chapter 9 will illustrate the current research progress of epitaxial lift-off (ELO) by demonstrating the device performance of both thin-film solar cell and the re-grown cell on the original bulk InP substrate after ELO. Chapter 10 will summarize the work of this thesis and point out some future directions for each of the demonstrated technologies.

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Chapter 1

Introduction

1.1 The motivation of deploying OADM in the WDM network

The original motivation of fiber optics communication is primarily to replace coaxial cables for long-haul communication. By adopting the optical amplifier and the scheme of wavelength-division multiplexing (WDM), the point-to-point long-haul lightwave system is capable of operating at the bit rate of 1 T bits/sec and regeneration span beyond 600 km. Figure 1.1 (a) shows the architecture of the long-haul optical network of fiber optic communication system in early days. Under this scheme, at each intermediate node, lightwave signals that travel in the backbone fiber are downloaded, converted into the electronic domain, regenerated, and re-transmitted into the backbone fiber. This network architecture is not only costly but also drastically limits the bandwidth. Therefore, it will be advantageous to the conventional communication system with a sophisticated optical switching and routing system, as shown in Figure 1.1 (b). By adopting optical add-drop multiplexers (OADM), the selected wavelength channels can be downloaded/uploaded at any intermediate node in the optical network while the unselected channels are unaffectedly passed through. Each node then communicates with its own local area network (LAN) with conventional time-division multiplexing (TDM) technology to achieve the mission of information exchange.

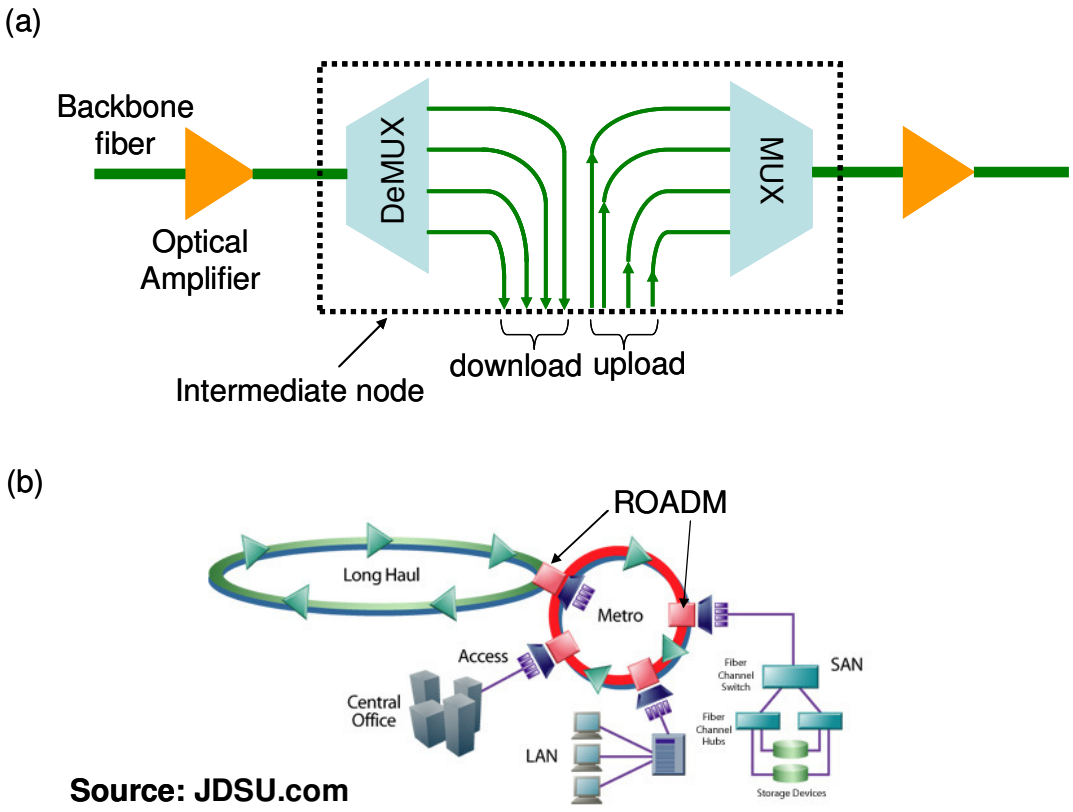

Fig. 1.1 *(a) Point-to-point fiber links for long-haul lightwave system (b) Architecture of the WDM network based on OXC and OADM (Source: JDSU.com)*

Depending on the flexibility of allocating wavelength channels, OADM can be classified as fixed-OADM (FOADM), which can only process the pre-determined wavelength channels, and reconfigurable-OADM (ROADM), which can upload/download any wavelength channel specified in real-time. Although FOADM is generally simpler and less expensive than ROADM, it is not able to fully utilize the transmission capacity of the fiber network because it cannot dynamically allocate the wavelength channels based on the real-time WDM traffic demand. As the emerging service applications, such as internet television service, continue to raise the internet

traffic volume, replacing FOADMs with ROADMs to ensure the provisioning and reconfiguration of the entire network will be an inevitable trend.

1.2 Review of the past technologies of ROADM

Numerous research efforts have focused on developing the ROADM. As shown in Figure 1.2, a commonly used technology for realizing wavelength add-drop is to combine fiber Bragg gratings (FBG) with optical circulators [1-2]. Basically, an optical circulator is a three-port device that allows light to travel at one direction. By incorporating the FBG at the intermediate port of the optical circulator, only a specific wavelength, determined by the FBG, is reflected to the drop port, while other WDM channels are transparently passed through. Typically, a FBG device has leakage of less than -40 dB at the Bragg wavelength, and reflection of less than -20 dB outside the Bragg wavelength [1]. Also, the Bragg wavelength of a FBG can be adjusted with applied stress or changing temperature, which make it suitable for making a ROADM with low insertion loss and crosstalk.

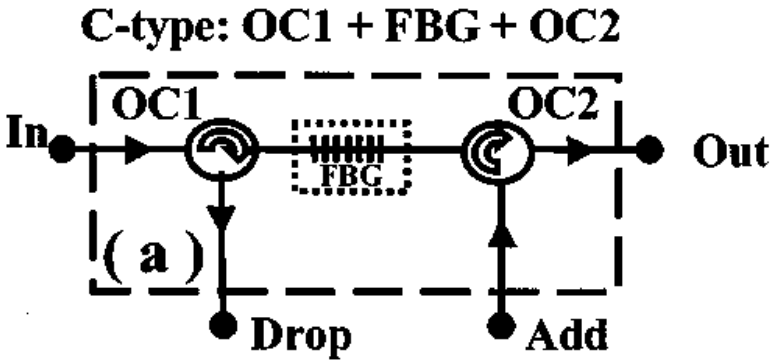

Fig. 1.2 *ROADM based on the combination of optical circulators and FBGs. [2]*

Another approach of wavelength add-drop is to apply a dielectric thin-film filter [3-5]. The dielectric thin-film filter is basically a cavity surrounded by a pair of dielectric mirrors. Ideally, this structure allows only one single wavelength to pass through, and reflects all of the other signals. Figure 1.3 (a) shows a schematic of a thin-film filter-based 2 x 2 add-drop unit [5]. This unit can selectively insert/download a wavelength channel by moving either the mirror or the tunable thin-film filter in the optical path. As shown in Fig 1.3 (b), the ROADM can be realized by cascading such multiple units. In general, the thin-film filter based ROADM usually suffers from high crosstalk, and therefore requires multicavity design to reconcile this weakness [3].

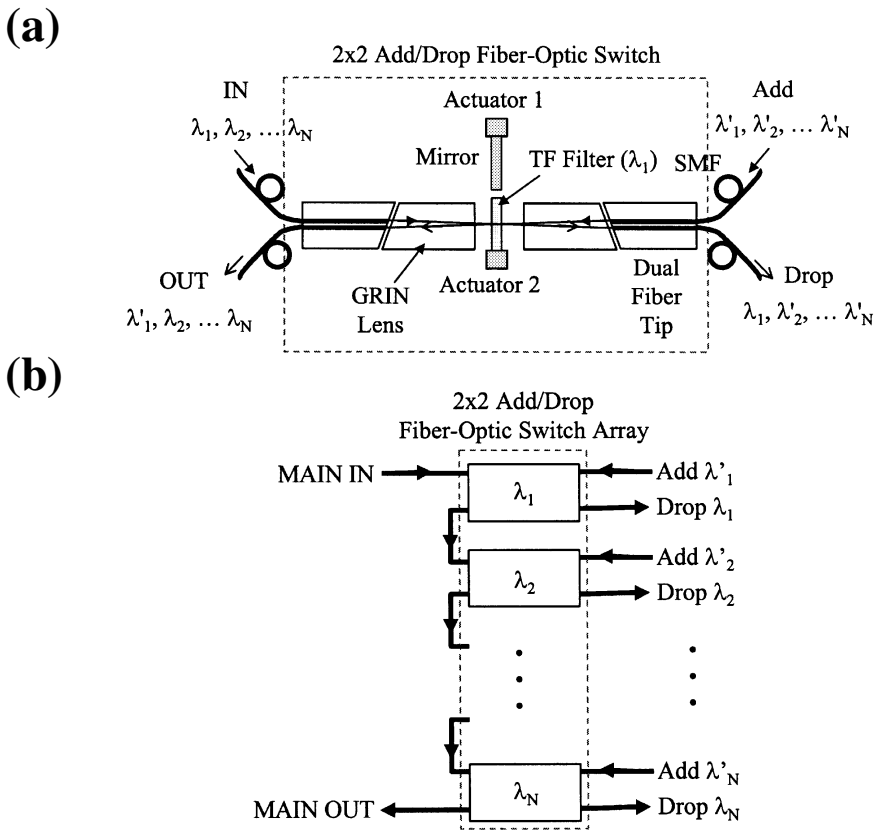

Fig. 1.3 *(a) Schematics of thin-film filter based add-drop unit [5]*
(b) Schrmatics of thin-film filter based ROADM [5]

The wavelength selective switch (WSS) is another state-of-art ROADM. The ROADMs within this category are implemented with free space optics, where a bulk diffraction grating is used to perform multiplexing/de-multiplexing, and the switching is achieved with a MEMS mirror [6-7]. Therefore, a WSS-based ROADM can potentially have the best insertion loss and crosstalk performance among all of the related ROADM technologies. Figure 1.4 presents a functional diagram of the wavelength selective switch-based ROADM, which exhibits a switching contrast ratio of 30 dB and insertion loss of less than 5 dB [6]. Moreover, as shown in Fig 1.5, the generalized WSS-based ROADM can not only drop a selected wavelength channel, but also can assigned any subset of the dropped wavelength channels to any one of the drop ports [8]. Despite these advantages, the WSS-based ROADM is not as compact or reliable as the other competing ROADM technologies.

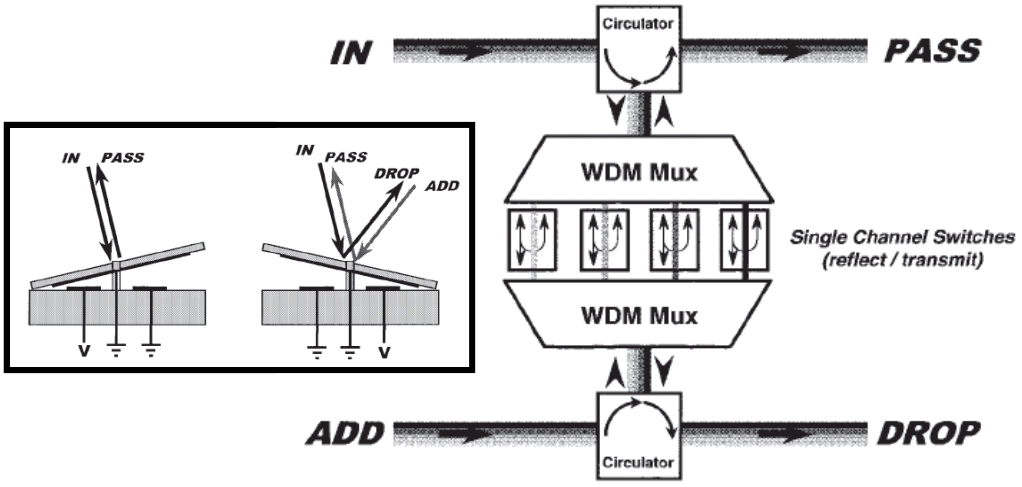

Fig. 1.4 *.The schematics of the WSS-based ROADM [6]*

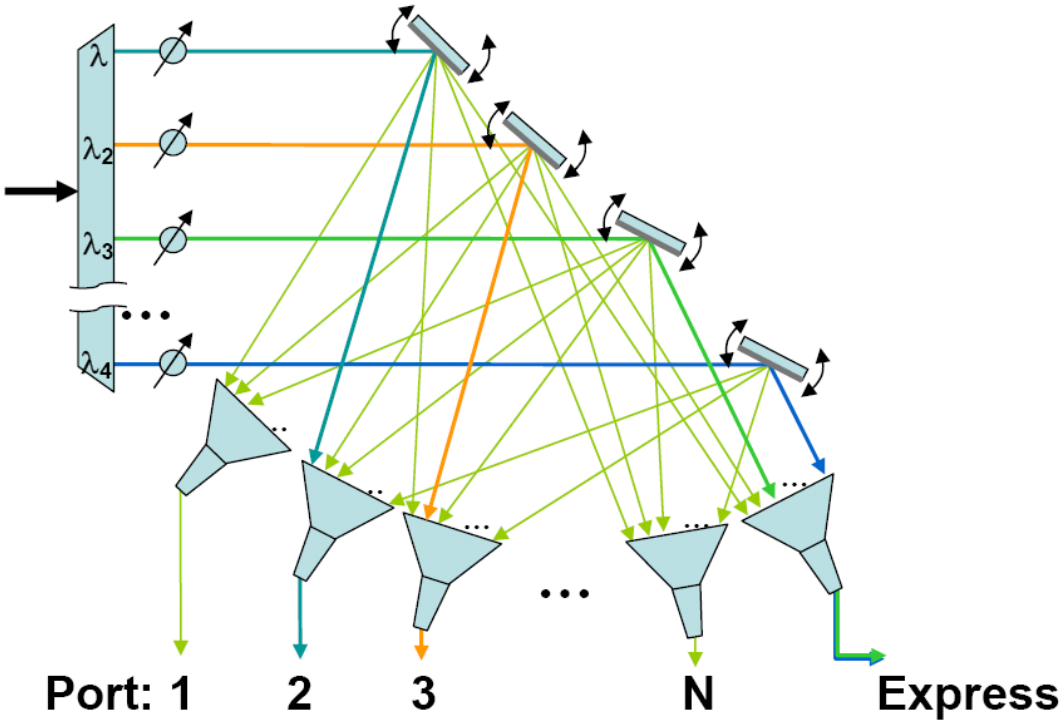

Fig. 1.5 *.The schematics of the generalized WSS-based ROADM [8]*

All of the previous ROADM devices have their own characteristic and advantageous. Nevertheless, independent of their operating principles, they all require multiple discrete optical components to perform the function of wavelength add-drop. Each discrete optical element requires sophiscated packaging which typically leads to low production yield. On the other hand, a compact planar lightwave circuit (PLC) technology provides an opportunity to realize complex photonic integrated system with high stability and low production cost [9]. Numerous PLC-based ROADMs have been demonstrated using silica, hybrid silica-polymer, and InP [10-12]. Silica-based PLC-ROADM typically exhibits -10 dB of insertion loss and more than -30 dB of crosstalk [10]. The power consumption of the silica-based PLC-ROADM can be further reduced

by performing chip-scale hybridization of silica multiplexer/de-multiplexer and polymer thermo-optic switches due to the higher thermo-optic coefficient of polymer than silica [11]. On the other hand, an InP-based PLC-ROADM demonstrated an insertion loss of -11 dB, and crosstalk of -20 dB [12]. Although the InP-based PLC-ROADM has inferior crosstalk to silica-based PLC-ROADM, it has the potential to ensure monolithically integrated active optical components to perform more complex optoelectronic functions, all on the same chip.

1.3 Functional description of a ROADM

The ROADM demonstrated in this thesis work is the InP-based PLC ROADM realized by combining the passive ROADM of ref [12] with active components, including a semiconductor optical amplifier and photo-detectors, all on the same InP substrate. Figure 1.6 presents a schematic of the monolithically integrated InP ROADM [13]. The WDM channels, simulated by an off-chip tunable laser, are coupled from the optical fiber into the waveguide of the ROADM chip, amplified by an on-chip semiconductor optical amplifier, and separated into different waveguides by a de-multiplexer. The user can electrically control the optical switches to route each wavelength channel to either the through ports or the drop ports, terminated by the integrated photo-detectors. If the light is routed to the through port, the individual wavelength channels are then combined by an on-chip multiplexer and are coupled to the external optical fiber output. On the other hand, there is another on-chip de-multiplexer at the add port to accept and separate the incoming new uploading WDM signals, supplied by off-chip tunable lasers. Some of the new WDM signals can be selectively routed to the through port by the same on-chip

optical switch array if the corresponding channels from the input port are dropped to the photodetectors.

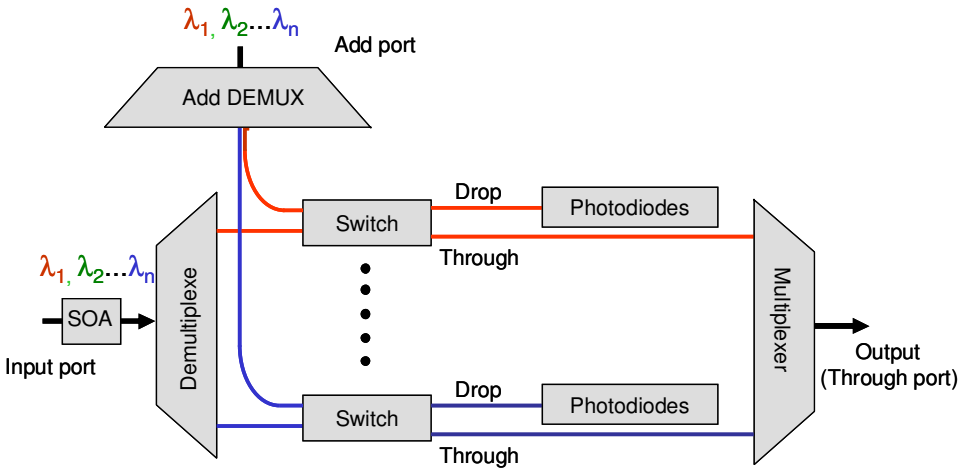

Fig. 1.6 *Schematics of the InP PLC-ROADM in this thesis work [13]*

The performance of an individual InP PLC-ROADM can be characterized by its speed, insertion loss, and optical crosstalk. The speed of the ROADM is determined by SOA, optical switches, the bandwidth of the integrated photodetectors at the drop port, and the on-chip tunable lasers at the add port. The insertion loss of a ROADM is represented in Fig 1.7, which is the qualitative transmission spectral response of a single ROADM at which the add-drop happens at the wavelength, λ_i [14]. In Fig. 1.7, the add/drop insertion loss is defined as $L_{c,ho}$, while the through insertion loss is represented by $L_{b,he}$. In general, the add/drop insertion loss is affected by the waveguide propagation loss and the contrast ratio of the optical switches. On the other hand, the through insertion loss is not only determined by the optical switches, but also mainly comes from the loss after passing through the multiplexer and de-multiplexer. In fact, the through insertion loss is the most critical parameter when deploying ROADMs in the ring network, because the light will experience multiples of such a loss when traveling in the network.

Nevertheless, this problem can be reconciled by deploying on-chip semiconductor optical amplifiers in the ROADM circuit.

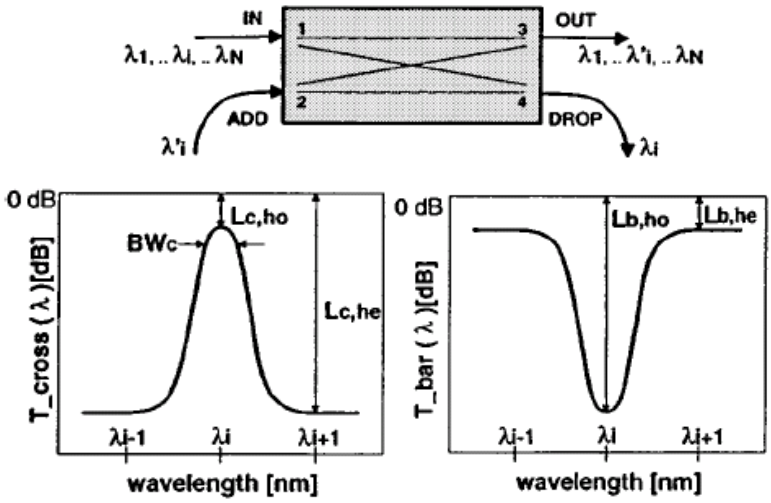

Fig. 1.7 *The functional schematics of a ROADM and the spectral response of an add-drop operation [14]*

Crosstalk is an important parameter characteristic of a ROADM device. In general, crosstalk in ROADMs results from internal reflections, switch leakage and multiplexer/de-multiplexer leakage [15]. The generalized leakage path of a ROADM device is shown in Fig 1.8 [16], where the solid lines labeled 1 to 3 show the intended routes within the ROADM circuit, while the dashed lines labeled 4 to 8 show the leakage paths. Here, depending on the phase correlation between individual signals, the crosstalk of a ROADM device can be further classified as either coherent or incoherent. For example, the interference between path 1 and path 5 is considered as the coherent crosstalk because both paths originate from the same light source. On the other hand, the signal from path 1 and path 4 has random phase relationship because they come from different light sources despite of the same wavelength, λ_{ad}.

To show the impact from either the coherent or incoherent crosstalk, we assume the electric field at the output port from path 1, 4, 5 is E_1 (t), E_4 (t) and E_5 (t) respectively. Each field can be represented as:

$$E_m(t) = E_m \exp[\, j(\omega t + \phi_m(t))] \qquad (1.1)$$

where m is 1,4, or 5 and $\phi_m(t)$ represent the phase of each field. Therefore, the total optical power, P_{out}, from the add port to the output port will be [17]:

$$P_{out} = \left|E_1^2\right| + \left|E_5^2\right| + 2\left|E_1\right|\left|E_5\right|\cos(\phi_1(t) - \phi_5(t)) \qquad (1.2)$$

Since E_1 and E_5 come from the same light source, E_5 is simply the delayed version of E_1.This implies that phase difference, $\phi_1(t) - \phi_5(t)$, is constant. Hence, P_{out} will maintain stability and therefore the coherent crosstalk does not result in noise to the system [15-17]. However, in the case of the interference between path 1 and path 4, the phase difference, $\phi_1(t) - \phi_4(t)$, will fluctuate randomly between 0 and 2π because E_1 (t) and E_4 (t) originate from two independent light sources. This fluctuation of P_{out}, ranging over the range of $\left|E_1 \pm E_4\right|^2$, is called phase induced intensity noise, and will introduce extra power penalty to the entire lightwave system [15-17].

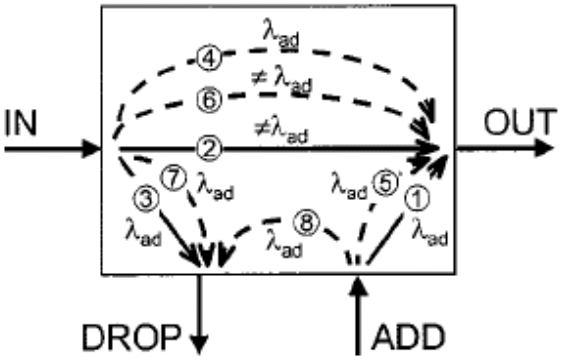

Fig. 1.8 *The intended routes, labeled as 1,2,and 3, and the leakage paths, labeled as 4 to 8 with a ROADM circuit [17]*

1.4 Asymmetric twin waveguide technology

The main task of this work is to demonstrate the InP-based PLC-ROADM which monolithically integrates the components of light-guiding, optical switching, multiplexing/de-multiplexing, light amplification, and light detection on the same chip. In the past, various technologies of photonic integration have been developed such as material re-growth [18-22], quantum well (QW) intermixing [23-25], selective area regrowth [26-29], and asymmetric twin waveguide technology (ATG) [30-31]. The photonic integration technology chosen here is ATG because it eliminates the need for material regrowth, and requires only standardized fabrication processes that are independent of a particular circuit configuration.

The evolution of ATG started from the twin-waveguide (TG) structure, introduced by Suematsu, et al [32]. Figure 1.9 is the typical TG structure and its mode profile, if implemented with the InP-based material system [30]. A TG structure basically supports two eigenmodes with near identical effective indices: one symmetric (even, ϕ_e) and one anti-symmetric (odd, ϕ_o). Due to interference between the modes, power will resonantly flow from one waveguide to the other with the characteristic length of [30]:

$$L_c = \frac{\lambda}{2(n_e - n_o)} \qquad (1.3)$$

where n_e and n_e are the effective indices of the even and odd eigenmodes. Photonic integration is achieved by designing the characteristic length to optimize the optical gain and light coupling efficiency between waveguides. Nevertheless, the characteristic length, L_c, is very sensitive to the composition and dimension of the waveguides. Inevitable run-

to-run variations from the epitaxial growth and device fabrication will significantly degrade the performance of the photonic integrated device [30].

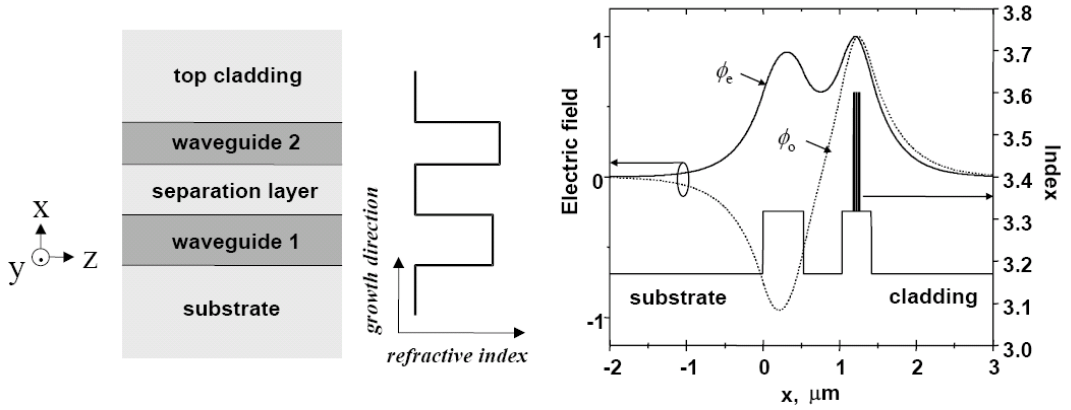

Fig. 1.9 *The structure of twin waveguide and its corresponding mode profile if implemented with InP-based material system [30].*

Instead of utilizing resonant power transfer to achieve light coupling, Studenkov, et al propose improved integration scheme, using an asymmetric twin waveguide structure [30, 33]. As the name implies, the ATG structure is similar to TG, except for significant differences in the refractive indices of the passive and active waveguides. Since the mode symmetry is broken, the resonance of the TG structure disappears. Figure 1.10(a) and Fig. 1.10(b) shows the refractive index profile and the ATG structure of the optical amplifier integrated with a passive waveguide [30, 33]. Here, the refractive index of the active waveguide, consisting of multiple quantum wells, is smaller than that of the passive waveguide. In this configuration, the even and odd modes will be unevenly split, with the odd (even) mode primarily confined in the active (passive) waveguide. Thus, the odd mode will have higher confinement factor than the even mode, leading to superior gain and reflectivity at the etched facet edge shown in Fig 1.10(b).

In the ATG structure shown in fig 1.10(b), the light is first coupled from the optical fiber into the passive waveguide. When the light enters the ATG region, it splits into even and odd modes, ϕ_e and ϕ_o , with the corresponding amplitude coupling coefficients, C_e and C_o, determined by their overlap integral with the eigenmode of the ATG waveguide, ϕ_p [30]:

$$C_{e,o} = \int_A \phi_{e,o} \bullet \phi_p \, dA \qquad (1.4)$$

. If we assume the optical fields at the entrance and exit of the ATG region are E_{in}, E_{out}, respectively, the total transmission ratio is [30, 33]:

$$\frac{E_{out}}{E_{in}} = C_e^2 \exp(\frac{\Gamma_e^{QW} gL}{2}) + C_o^2 \exp(\frac{\Gamma_o^{QW} gL}{2}) \exp(i\Delta k \cdot L) \ , \qquad (1.5)$$

where g is the gain of the MQW, L is the length of the ATG semiconductor optical amplifier, $\Gamma_{e,o}^{QW}$ are the confinement factors for the even/odd modes, and $\Delta k \cdot L$ is the phase shift between the even mode and odd mode. Since the odd mode has a higher confinement factor, the odd mode will eventually dominate the output power with increasing L. Hence, the output-to-input power can be approximated by [30, 33]:

$$\frac{P_{out}}{P_{in}} \approx C_o^4 \exp(\Gamma_o^{QW} gL) \qquad (1.6)$$

Therefore, by applying ATG structure, it is possible to integrate the active components with the passive waveguide on the same chip. Comparing to the TG structure, ATG is immune from variations in epitaxial growth and fabrication, and therefore provides reliable photonic integration of most optical components on the same chip.

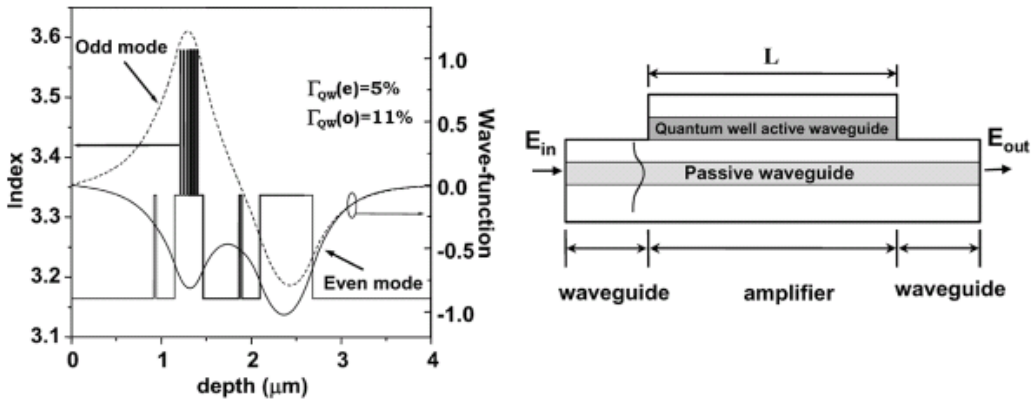

Fig. 1.10 *(a) The refractice index profile of the ATG structure [30]*
(b) The structure of ATG semiconductor optical amplifier integrated with passive waveguide based on the epitaxial layer shown at (a) [30]

Despite the robust photonic integration scheme provided by the ATG structure, coupling losses at the active-passive waveguide facets are presented [30]. To minimize loss when light is transferred between active and passive waveguides, the ATG structure is upgraded by incorporating tapered couplers [34], as shown in Fig 1.11. Here, the untapered region of the upper active waveguide is chosen to have larger effective index than those of the lower passive waveguide. The high effective index difference between both waveguides confines the even mode primarily in the untapered active waveguide. In the tapered region, the effective index of the active waveguide decreases as the taper width shrinks. As the effective index of the active waveguide approaches the lower passive waveguide, the light is gradually transferred to the passive waveguide via resonant coupling before reaching the end of the taper. The same coupling scheme also applies if light is transferred from the passive waveguide to the active waveguide. By adopting resonant or adiabatic taper, nearly lossless optical transfer can be achieved [2, 30]. Various photonic devices have been demonstrated with such an integration scheme

[35-44]. In this thesis, the InP-based PLC ROADM will also be implemented by applying this technology.

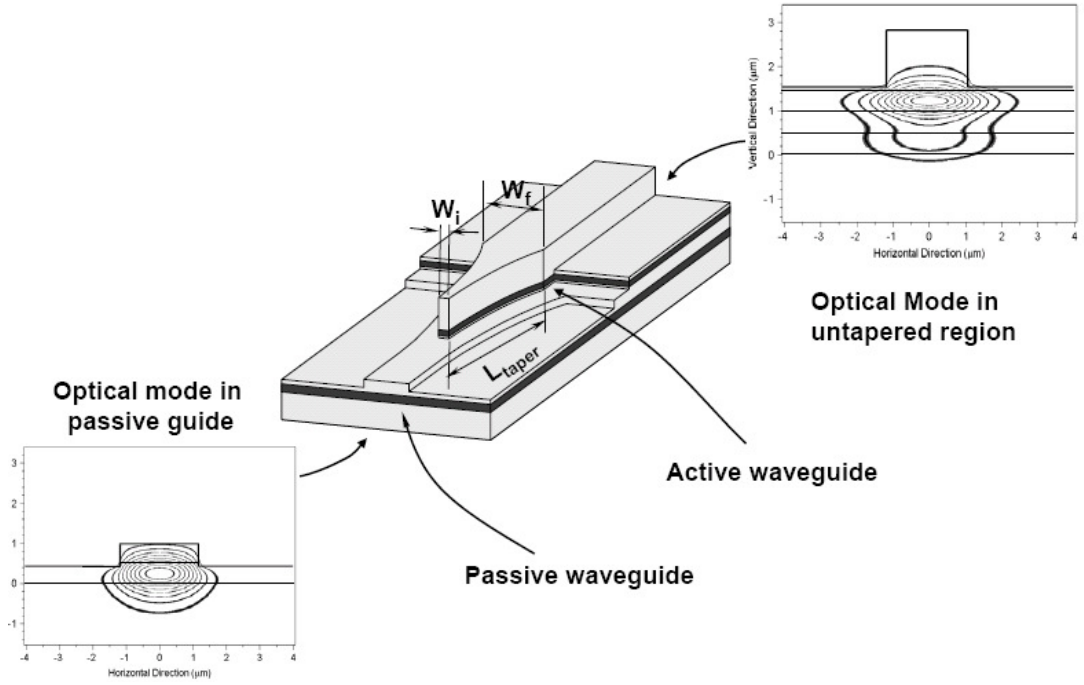

Fig. 1.11 *The illustration of ATG structure with taper coupler [30,34]*

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Chapter 2

2 x 2 optical switch & arrayed waveguide grating

2.1 Introduction

In this chapter, we will present the passive components for the ROADM system which will be responsible for routing WDM signals in the photonic circuit. The multiplexer/de-multiplexer is implemented with array waveguide gratings (AWGs) while Mach-Zehnder interferometer (MZI) optical switches are used for space-switching each individual wavelength channel inside the ROADM. The prior art of the optical switches will be first introduced before the detail descriptions of the optical switch in this work, which exhibits an on-off contrast ratio of (21±2) dB and a propagation loss of (3±2) dB. The 5-channel multiplexer/de-multiplexer in this work simply follows the design principles of standard AWG and has the characteristics of channel spacing of 1.8nm, non-uniformity of 2 dB, and crosstalk of –15±2dB dB. These passive components will share the same epitaxial layer structure together with the passive waveguide of the ROADM demonstrated at chapter 4.

2.2 Prior art of optical switch

The optical space switch plays an important role for routing the WDM traffic in the fiber optics network [1]. To be useful for photonic integration, the optical switches need to be compact, low loss, high speed, low power consumption, and have a high on-off ratio [1]. One simple example is to utilize a single Y-junction waveguide with carrier injection to achieve optical space switching [2]. However, such devices constantly

require equal electrical power in both the ON and OFF states to avoid splitting the signal between output arms. Another way of realizing optical switching is to integrate semiconductor optical amplifiers (SOAs) with the waveguides to either transmit or block the light by adjusting the current injection level into the SOA [3]. The major drawback of such SOA-based switches is the variation of gain with injection signal, which results in signal distortion and reduced on-off ratio [1]. On the other hand, optical switches utilizing the Mach-Zehnder interferometer (MZI) architecture, which allows for the independent optimization of the mode-coupling and phase-shifting regions [1], can potentially reduce the complexity and the area of the photonic integrated circuit. Using Y-junctions as optical beam splitters and combiners with an electric field applied to the waveguides between Y-junctions is the most straightforward way to implement MZI optical switch [4]. However, an N x N channel switch would involve multiple Y-junctions, which inevitably increase the layout complexity and therefore the system manufacturing cost. In contrast to that Y-junction configuration, the multimode interference (MMI) coupler is accepted as an efficient mode-coupling element in the MZI structure due to its compactness, tolerance to polarization variations, and wavelength independence [5]. One common example of a MMI-based optical switch is to apply the electro-optical effect to adjust the refractive index of waveguides between MMI couplers [6]. On that case, the length of the electrodes must be large (6mm) to induce the requisite phase change.

2.3 The design and fabrication of 2x2 optical switch

Comparing to prior art, in this work [7], we demonstrate a 2x2 switch with compactness and low power consumption that uses carrier injection induced refractive index changes to modulate the response of a pair of multimode interference (MMI) couplers, which are connected in the MZI configuration. The optical switch, shown in Fig. 2.1, includes two series-connected MMI couplers, with metallization on one of the access arms located between the MMIs. The switch has input ports, A and A', and outputs, B and B'. When the input is at A, B is the BAR port and B' is the CROSS port, and vice versa when the input is at A'. Both MMI couplers split the input optical fields equally at their output arms with a phase difference of $\pi/2$ [5].

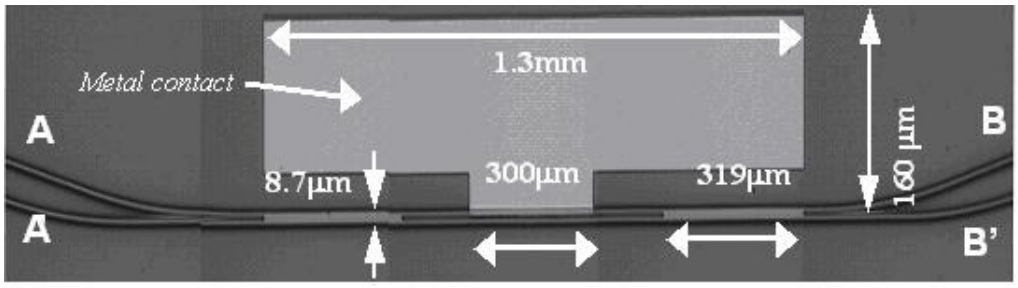


Fig. 2.1 *Micrograph of the optical switch with related dimensions and ports.*

When the switch is in the OFF state and the input is at A (A'), no current flows in the access arm and the light is transferred to the CROSS port B' (B) due to constructive interference at that port and destructive interference at the BAR port B (B') [5]. When a given current density, J, flows through the access arm, the corresponding carrier injection density, n, is governed by both the radiative and non-radiative recombination:

$$J = qd(An + Bn^2 + Cn^3) \qquad (2.1)$$

where d is the thickness of the access arm, and A,B,C represent the coefficients for the radiative, non-radiative and Auger recombination rates, respectively. In the so-called "band-filling effect", injected free carriers will fill the edge of the conduction and valence bands, leading to a decreased near band-edge absorption coefficient, $\Delta\alpha$ [8]:

$$\Delta\alpha(E) = C \cdot \frac{\sqrt{E - E_g}}{E}(f_v(E) - f_c(E) - 1) \ . \qquad (2.2)$$

Here, C is a constant related to effective mass of carriers and refractive index of the material, E is the photon energy, E_g is the bandgap energy, and f_v / f_c represents the Fermi Dirac distribution function for holes and electrons, respectively. Through the Kramers-Kronig relation, the corresponding change of the refractive index can be induced from $\Delta\alpha$ [8]. In addition to band-filling, photon absorption moves free carriers to a higher energy state within the band, which results in a corresponding refractive index change, called the plasma effect [9]. The plasma effect can be modeled by Lorentz oscillator model:

$$m\frac{dx^2}{dt^2} + m\gamma\frac{dx}{dt} + m\omega_0^2 x = -qE \qquad (2.3)$$

where x is the displacement of the free carrier from its equilibrium position, m is the mass of the free carrier, γ represents the damping force, ω_0 represents the restoring force, and E is the external electric field. In (2.3), since the injected electrons and holes are considered as free carriers, the restoring force, ω_0, is zero. Introducing $E = E_0 e^{i\omega t}$, and $x = x_0 e^{i\omega t}$, where ω is the frequency of the incoming electric field (photon), into (2.3), we get

$$x_0 = \frac{-q E_0 / m}{-\omega^2 + i\omega\gamma} \ . \qquad (2.4)$$

From (2.4), the individual dipole moment can be calculated, and therefore the polarization, P, is:

$$P = N(-qx) = \varepsilon_0(\chi' + i\chi'')E \qquad (2.5)$$

where N is the number of free carriers per volume, and χ' and χ'' represent the real part and the imaginary part of the electric susceptibility. The refractive index, n, can be deduced from electric susceptibility, and therefore the refractive index change due to the plasma effect is:

$$\Delta n_{plasma} = \frac{-Nq^2}{2n_r m\omega^2 \varepsilon_0} \qquad (2.6)$$

where n_r is the refractive index in the absence of carrier injection. Combining the band-filling and plasma effects, the total refractive change Δn_r can be calculated. When Δn_r is sufficient to cause a π-phase shift, the light is routed to the BAR port B (B') resulting in space switching of the signal.

The device is based on InGaAsP grown by gas source molecular beam epitaxy on an n-type (100) InP substrate. The detailed growth condition is described in [10]. The epitaxial structure along with the doping concentration of each layer is given in Table 2.1. The layers form a p-i-n diode, with an n-type region formed by the S-doped InP substrate and a Si doped InP buffer layer. The intrinsic region consists of undoped layers of InGaAsP (with energy gaps E_g =1.18eV) placed between InP layers, and the Be-doped p-type region is formed by the top 0.15μm thick InP and 0.2μm thick InGaAsP (E_g =1.03eV) cap layers. Using this

Material	Thickness	Doping	Function
N-InP	120μm	S	Substrate and N-contact
InP	500nm	Ramped Si $2x10^{18}cm^{-3}$ to $2x10^{17}cm^{-3}$	N-type buffer
InP	600nm	Undoped	Waveguide layer
InGaAsP (E_g =1.18eV)	600nm	Undoped	Waveguide layer
InP	600nm	Undoped	Waveguide layer
InGaAsP (E_g =1.18eV)	300nm	Undoped	Waveguide layer
InP	450nm	Undoped	Waveguide layer
InP	150nm	Ramped Be $1x10^{17}cm^{-3}$ to $1x10^{18}cm^{-3}$	P-type waveguide layer
InGaAsP (E_g =1.03eV)	200nm	Ramped Be $1x10^{18}cm^{-3}$ to $6x10^{18}cm^{-3}$	P-contact

Table 2.1 *Epitaxial layer structure of optical switch*

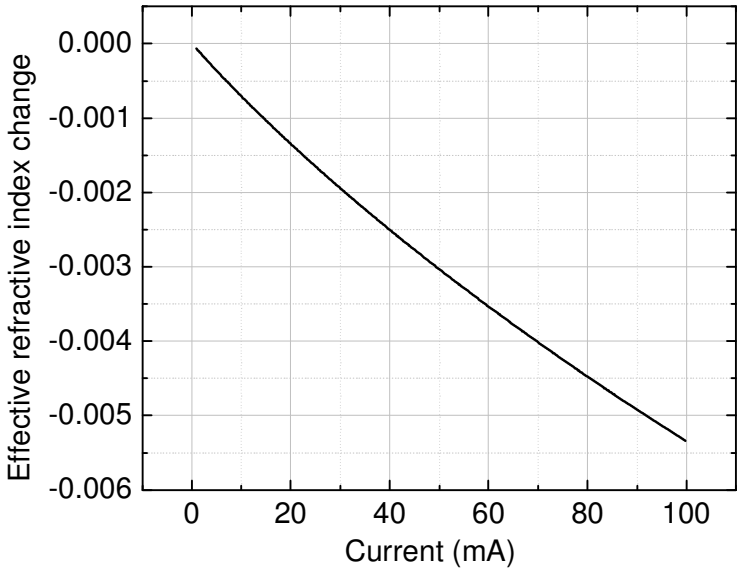


Fig. 2.2 *Refractive index change as a function of current for 300μm long and 3μm wide electrode region*

structure, the 3μm width of the input and output access waveguides is designed for high-fiber coupling and low birefringence (Δn_r <3x10^{-4}). Due to interspersing of InGaAsP (E_g =1.18eV, refractive index n_r =3.25) and InP (n_r =3.17) layers, this single-mode waveguide has a "diluted" design with an effective refractive index of n_r =3.1932 for transverse magnetic (TM) and n_r =3.1935 for transverse electric (TE) polarizations. For this epitaxial structure, the refractive index as a function of current, shown in Fig 2.2, was calculated from the previously described model. Using a 3D beam propagation model [11], complete switching of light with λ=1550nm between ports B and B' will require Δn_r = –0.003, which is predicted to be obtained at a current of I=45mA. The phase change stays within (π±0.1) rad in the wavelength range from λ=1520nm to 1580nm, resulting in low wavelength sensitivity of the switch.

Fabrication begins by plasma enhanced chemical vapor deposition of a 300nm thick layer of SiN_x in NH_3:N_2:SiH_4 (40:360:175) at 300^{0}C. This layer is used as a mask during reactive ion etching of the semiconductor in 1:7 CH_4:H_2 to form the MMI and waveguide patterns. A second, 500nm thick layer of SiN_x is deposited for passivation and planarization. The nitride on the top of the ridge is etched, followed by e-beam deposition of p-metal (Ti-Ni-Au) at an angle of 45^0 to avoid discontinuities in the metal coverage over the ridge. This is followed by lift-off and annealing at 425^{0}C for 30s. The substrate is lapped to ~120μm thickness, and then is coated with n-metal (Ge-Au-Ni-Au) and annealed at 360^{0}C for 90s.

2.4 Characterization of the 2x2 optical switch

The switch was mounted on a thermoelectric cooler to facilitate measurements at temperatures ranging from 16°C to 64°C. For optical testing, lensed single mode fibers were used to launch both TE and TM light through port A, and the output was collected at both B and B'. The waveguides are bent at an angle of 7° to avoid reflections back into the waveguides. The loss due to coupling from the fiber to the waveguide for one facet is 5dB [12], and for the second facet it is 8dB, the difference arising due to the different radii of curvature of the two lensed fibers used. Thus, the total fiber-to-chip coupling loss is approximately 13dB.

Figures 2.3 and 2.4 show the normalized light output from ports B and B' for TE and TM modes, respectively. The data were collected at T=24^{0}C and at λ=1550nm. The effective refractive index change corresponding to a given current density was used to obtain the theoretical fits [11], which are also plotted in Figs. 2.3 and 2.4 (solid lines). The difference in the outputs at the CROSS port in the OFF state and the BAR port in the ON state for TE and TM polarizations is <2dB. The contrast ratio for both polarizations is >16dB at 24^{0}C for this device. The on-chip propagation loss, which is the excess loss after taking into account the fiber-to-chip coupling loss, is (3±2) dB. We obtain similar results to those shown in Figs. 2.3 and 2.4 with the light launched into port A'. The error bars take into account fluctuations in fiber alignment due to temperature changes and mechanical vibrations of the setup.

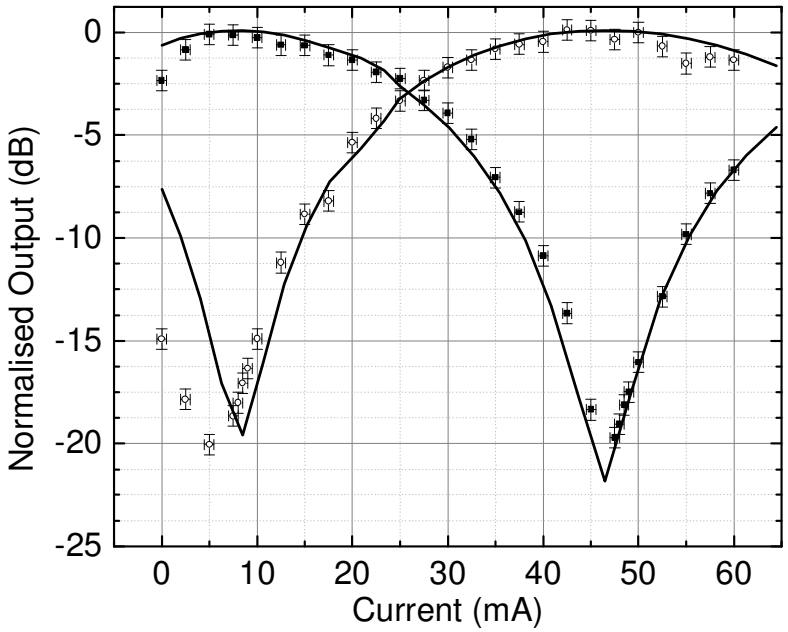


Fig. 2.3 *The switching of light as a function of input current for TE polarizations. Filled rectangles indicate cross port and empty circles indicate bar port output.*

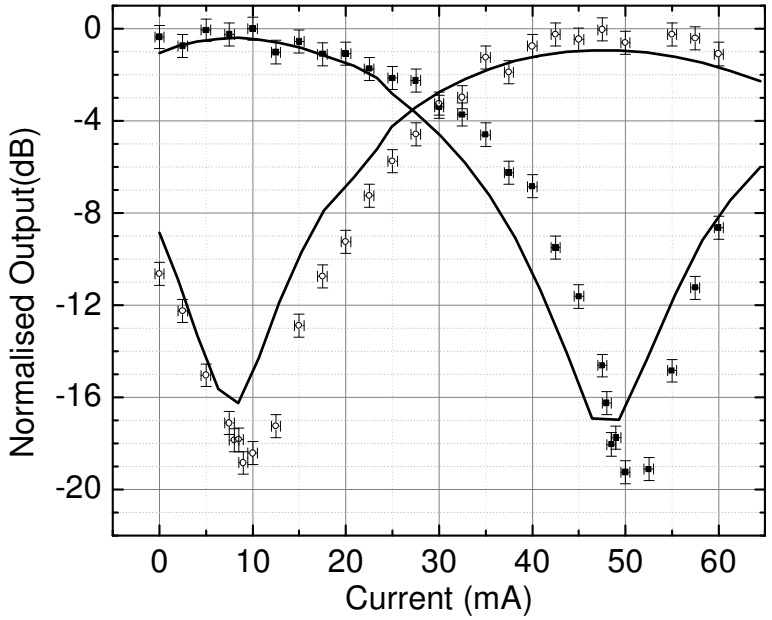


Fig. 2.4 *The switching of light as a function of input current for TM polarizations. Filled rectangles indicate cross port and empty circles indicate bar port output.*

Figure 2.5 and its inset show the wavelength dependence of the insertion loss and the contrast ratio of TE mode, respectively. For both modes, the insertion loss stays within 3 dB, and the contrast ratio remains constant from λ= 1520nm to 1580nm, which is consistent with the wavelength independent nature of the MMI coupler [5].

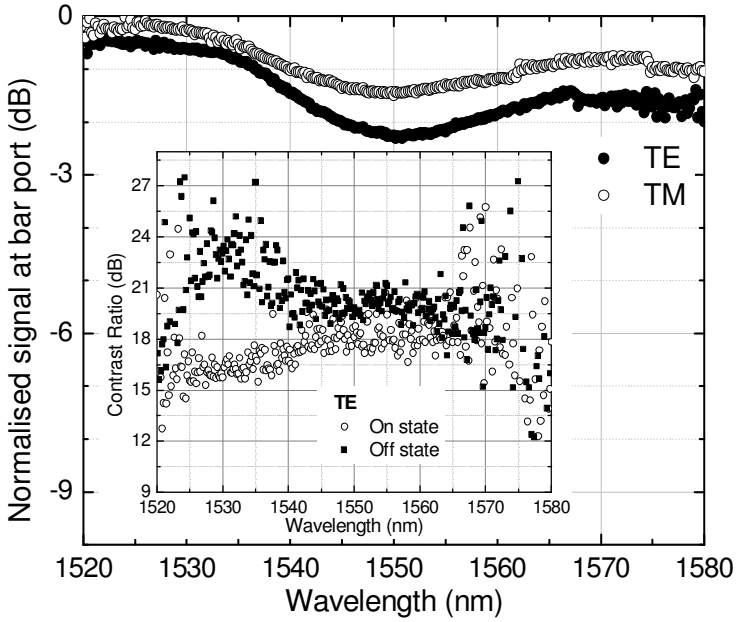


Fig. 2.5 *Transmission at bar port in ON state for both polarizations versus wavelength. Inset: Contrast ratio versus wavelength for both states for TE polarization*

The dark current-voltage (I-V) characteristics of the device are shown in Fig. 2.6. From these data, the voltage for OFF state, corresponding to I=(7±2)mA, is V_{Off} =(2.3±0.12)V, and for ON state, corresponding to I=(49±3)mA, is V_{On} =(3.3±0.06)V. Thus, the voltage swing needed for on-off operation is ΔV_{π} = (0.9±0.2) V, and the maximum power dissipated by the switch is P_{max}=160mW. The parasitic series resistance from the I-V characteristics is approximately 17Ω. Note that the contrast ratio in the OFF state is maximum at a current slightly larger than 0mA. This is due to the asymmetry in

the widths of the two waveguides separating the MMIs, which arises during lithography and etching.

The measured capacitance of the switch is (24±2)pF. By including contact resistance of 17Ω and a 50Ω load, it gives a resistance-capacitance (RC) time constant of 1 ns, shorter than the typical carrier recombination lifetime of 5-10ns [13], which therefore provides the switching bandwidth limitation in this device.

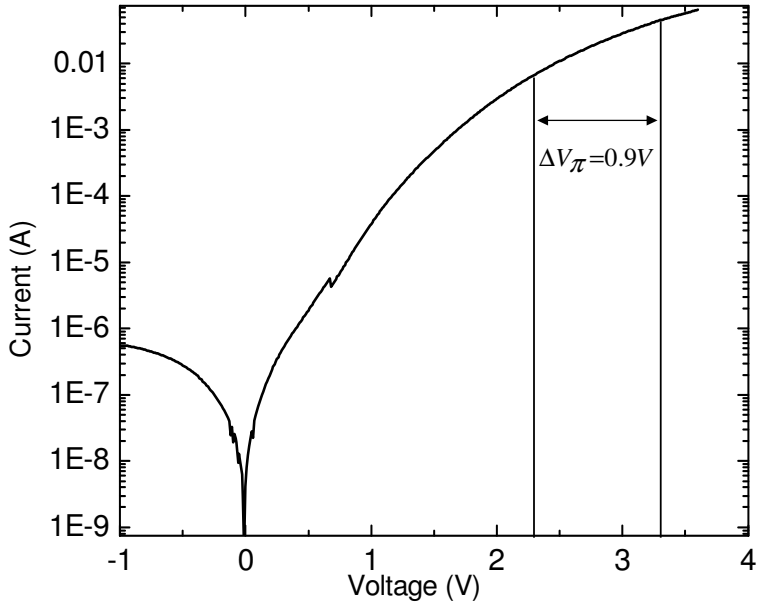


Fig. 2.6 *IV characteristics of the switch showing the OFF and ON state voltage. (OFF state voltage is (2.3±0.1) V. ON state voltage is (3.3±0.1) V.)*

2.5 Design and testing of the AWG

The multiplexer (MUX) and de-multiplexer (DEMUX) are the key components in the ROADM circuit. Various technologies have been used to implement MUX/DEMUX, including grating-based [14], [15], MZ-based [16], and phased-array based devices [17]. From the lightwave system design point of view, the MUX/DEMUX must be compact, robust, and monolithically integratable with the other optical components. Concave grating devices typically need vertical reative ion etch (RIE) to define the grating, and

therefore, they have lower tolerance for variations. MZ-based devices usually need multiple serial connections of couplers to separate/combine wavelength channels, and thus inevitably require large chip area. On the other hand, phased-array based devices, also termed arrayed waveguide gratings (AWG), can be implemented with conventional waveguide technology, and have more tolerance to fabrication variations. As shown in Fig. 2.7, an AWG device consists of free propagation regions (FPR) and an array of bent waveguides that connects the couplers. The length of each array waveguide is chosen such that the phase shift of the central wavelength between adjacent arrayed-waveguides is equal to a multiple of 2π. Thus, the phase of the central wavelength is the same at the output aperture as at the input aperture, thereby enables re-focusing on the central output waveguide of the image plane. Any variations in the wavelength of propagating light would introduce additional phase change at the output aperture and therefore tilt the focus spot from the center of the image plane. By deploying multiple properly spaced output waveguides at the image plane, each wavelength channel can be separately collected. The detailed operation principle of the AWG can be found in [17].

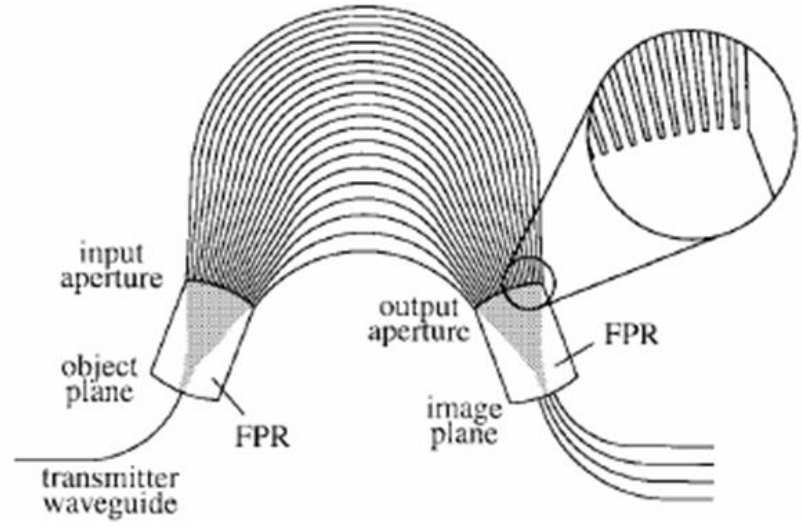
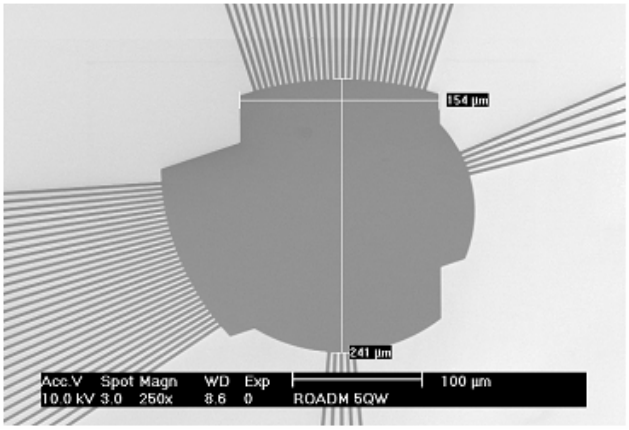


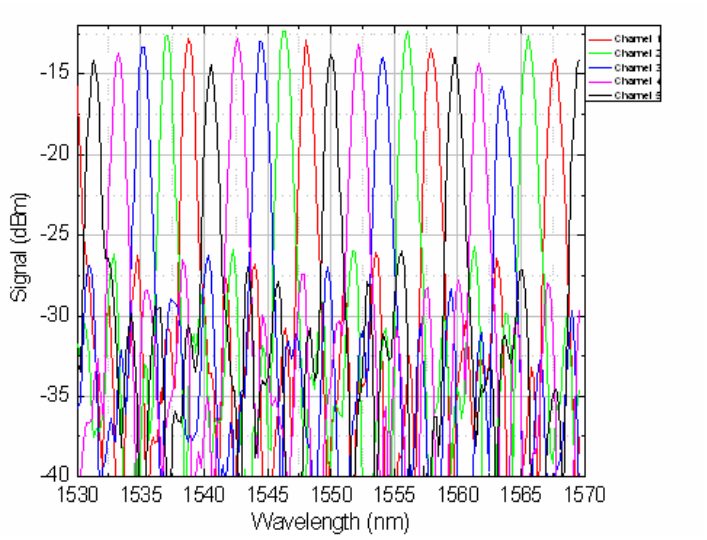
Fig. 2.7 *Schematic of arrayed-waveguide grating device[17]*

In this work, we simply choose the standard AWG as the MUX/DEMUX in our ROADM circuit. Our AWG is designed to have five input/output channels, wavelength channel spacing of 2nm, and free spectral range of 10nm. It has 30 arrayed-waveguides with the minimum bending curvature of 700μm and total size of 3mm x 4mm. Since the ROADM circuit will need two de-multiplexers to separate the incoming WDM channels from the input and add port, it is inevitable that both AWGs will have overlapping free propagation region (FPR). The fabrication procedure is similar to optical switch described above, excluding the metallization step. The detailed epitaxial layer structure is identical to the passive fiber waveguide of the SOA-PIN device described in the next chapter. Figure 2.8 (a) is a scanning electron microscope (SEM) image detail of the final AWG device coupler region.

Figure 2.8 (b) shows the transmission spectrum of the AWG at the four output ports for wavelengths ranging from 1530nm to 1570nm. The insertion loss is 12±2dB, while the channel non–uniformity is 2dB. The actual wavelength spacing is 1.8nm exhibiting a crosstalk of –15±2dB. The insertion loss is contributed by both the non-zero spacing of the arrayed-waveguides at the aperture of the FPR, and the propagation loss due to free carrier absorption from the Si-doped InP layer at the top of the passive waveguide. Although reducing the gap between the arrayed-waveguide aperture can further suppress the insertion loss, more photoresist residues are likely to fill in the gap after the photolithography, and therefore cause inhomogeneous filling after the dry etching process. These inhomogeneous filling disturbs the effective index of the arrayed-waveguides, and therefore can increase the crosstalk [17].



(a)



(b)

Fig. 2.8 *(a) The SEM image of the AWG with overlapped FPR*
(b) The transmission spectrum of the AWG

2.6 Summary

In this chapter, we have modeled, designed and demonstrated a simple and compact, 2x2 optical switch and a standard five-channel AWG. The optical space switch has an on-off contrast ratio of (21±2)dB for both TE and TM polarizations at both the BAR and CROSS ports and over the wavelength range from λ=1520nm to 1580nm. The

polarization sensitivity is less than 2dB for the TE and TM modes. Due to the waveguide routing issue in the ROADM circuit, the AWG devices are fabricated with overlapping FPR. It exhibits the insertion loss of 12±2dB, non-uniformity of 2dB, and crosstalk of -15±2dB. Both the switch and AWG will be integrated in the ROADM circuit demonstrated in Chapter 4.

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Chapter 3

Monolithically integrated optical receiver

3.1 Introduction

To compensate for the insertion loss, the ROADM circuit in this work monolithically integrates the p-i-n photodiodes at the drop port, and the semiconductor optical amplifier (SOA) at the input port. This chapter describes a prototype monolithically integrated optical receiver to show the feasibility of simultaneously integrating multiple active components in the single photonic circuit. Here, we integrate a SOA and a p-i-n photodetector based on asymmetric twin-waveguide (ATG) technology. Multiple quantum wells with 1% compressive strain are used for both optical amplification and detection. The device has a peak external responsivity of 8.2±0.4 A/W (~ 9dB fiber-to-detector gain), and a 3dB optical bandwidth of 11±1 GHz, equivalent to a 265 GHz gain-bandwidth product. The efficient coupling of light between individual optical components is achieved by a lateral adiabatic taper that reduces the fabrication complexity. Comparing to previous reported integrated receiver, which require either material regrowth or complex fabrication steps, this work represents a considerable simplification over previously demonstrated high performance integrated optical receivers.

3.2 Design and fabrication of integrated optical receiver

The motivation of integrating SOA into the ROADM circuit is to reduce the insertion loss and increase the sensitivity of the photodiodes at the drop port. What high

sensitivity optical receivers often consist of optical preamplifier embedded with photo-detector. For example, erbium-doped fiber amplifiers enable at least 15 dB improvements in the sensitivity of the optical receiver [1], [2]. To further simplify the packaging complexity and reduce the total system cost, efforts have been focused on realizing monolithically integrated optical receivers [3-5]. However, these technologies either require materials regrowth or complex fabrication steps. Here [6], we demonstrate a high performance and significantly simplified monolithically-integrated optical receiver based upon the ATG platform.

Figure 3.1 shows a schematic of the receiver, consisting of the combination of an SOA and p-i-n photodetector (SOA-PIN). The SOA consists of a ridge waveguide gain section bound by two tapers, while the PIN detector, with a single taper, has an absorbing region consisting of the same compressively strained multiple quantum well material used to generate gain in the SOA. The optical signal input from the fiber is coupled into the circuit via a passive waveguide [3]. The light propagating in the passive waveguide is transferred to the SOA ridge via the adiabatic taper coupler [7]. Following propagation through the traveling wave optical amplifier, the light is then transferred back to the dilute waveguide through the second taper coupler. For detection, the light is transferred into the tapered absorbing region.

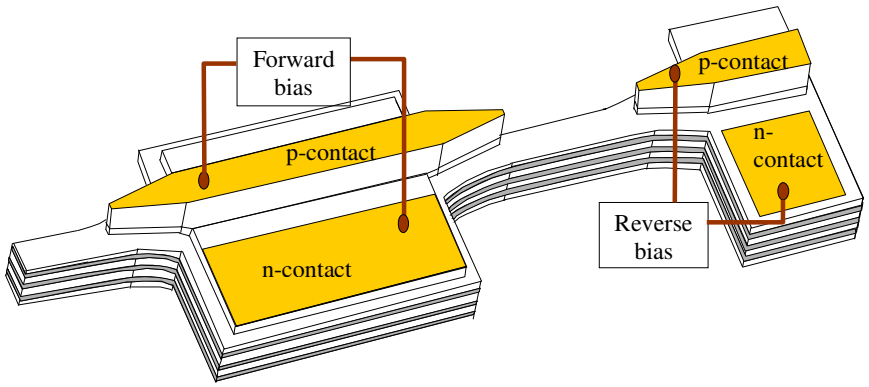

Fig. 3.1 *Three-dimensional schematic view of the integrated optical receiver*

The epitaxial structure of the device is grown by gas source molecular beam epitaxy on a (100) S-doped InP substrate. The detailed growth condition is stated in [10] at Chapter 2. The lightly Si-doped dilute waveguide consists of three InGaAsP (with a bandgap energy of E_g = 1.03eV) layers of thickness 0.165µm, 0.18µm and 0.195µm, interleaved with two 0.45µm thick InP layers. The gain/detection material consists of five, 1% compressively strained, 135 Å thick InGaAsP (E_g ~ 0.67eV) QWs separated by 230Å thick InGaAsP (E_g = 1.03eV) barriers. This structure is sandwiched between two, 120nm thick InGaAsP layers (E_g = 1.03eV) that complete the separate confinement heterostructure. Finally, a 1µm thick Be-doped InP cladding layer is grown on top of the active region, followed by a 0.1µm thick $In_{0.53}Ga_{0.47}As$ Be-doped ($1x10^{19}cm^{-3}$) contact layer. The cross-sectional SEM image of the epi-structure of the multiple quantum wells a

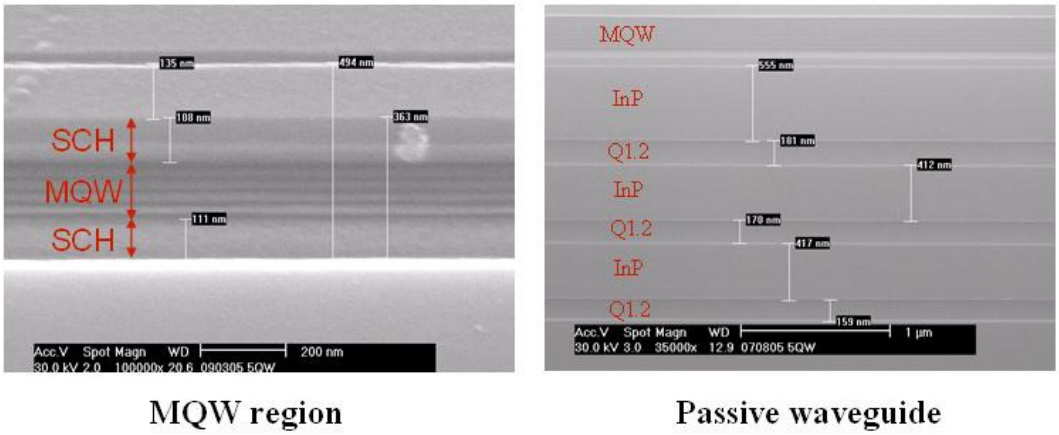

Fig. 3.2 *Cross-sectional SEM image of the epi-structure of the multiple quantum wells and the passive waveguide in SOA-PIN.*

The fabrication of the receiver is similar to that conventionally used for ATG components [3]. The wafer is first coated with 300nm of SiNx using plasma-enhanced chemical vapor deposition. As shown in Fig 3.3(a), the shape of the taper is defined using photolithography followed by the subsequent reactive ion etching (RIE) of $In_{0.53}Ga_{0.47}As$

contact layer and wet etching of InP cladding layer with SiNx as the mask. The shallow ridge, deep ridge of the active waveguide, and the passive waveguide are then defined by photolithography and RIE, shown in Fig 3.3(b) and (c), respectively. The motivation for applying shallow ridge structure to the active waveguide is to avoid light scattering and surface recombination from the damaged ridge sidewall created by RIE. Finally, Fig. 3.3(d) shows the entire device after planarizing with Benzocyclobutene (BCB) and coating metal contact.

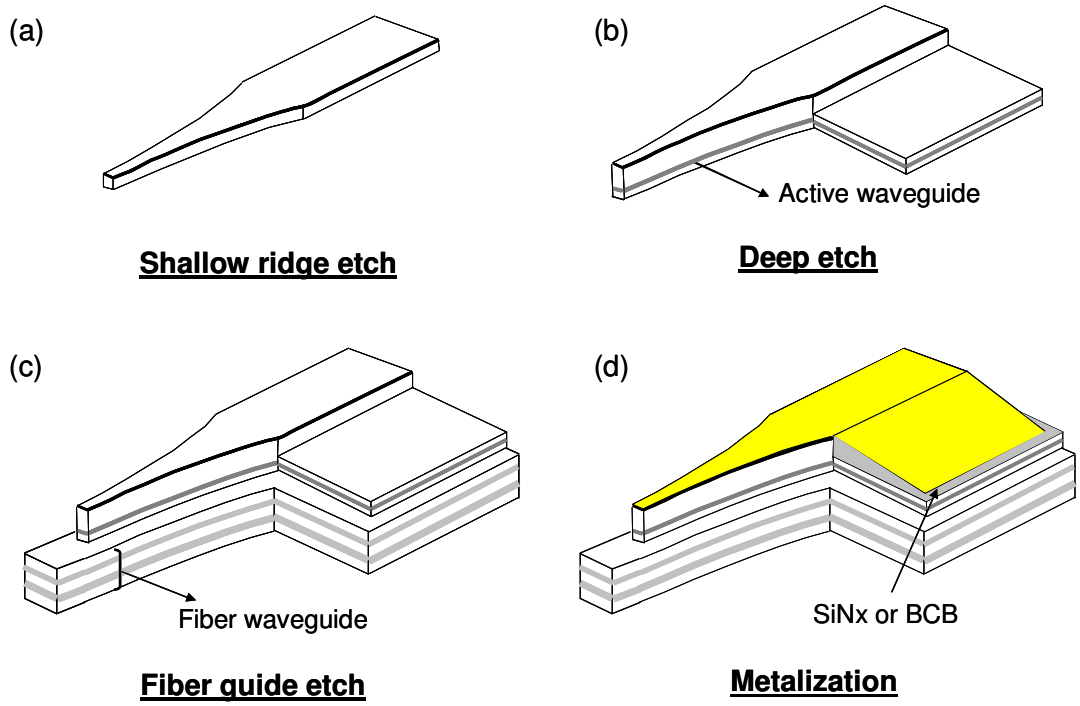

Fig. 3.3 *Schematics of fabrication steps of SOA-PIN. [8] (a) define the shape of taper with optical lithography and R.I.E. (b)define the area of active waveguide with optical lithography and wet-etching (c) define the area of passive waveguide with optical lithography and R.I.E. (d) define the metal contact for the active waveguide.*

Here, the dilute waveguide width of 4µm is chosen for efficient fiber coupling [7]. The corresponding adiabatic taper length used for the SOA is 210µm long, varying from 1µm at the tip to 3.5µm at the base. The detector taper is 150µm long with a width variation similar to that used for the SOA tapers. The SOA ridge is 1mm long by 3.5µm wide, while the detector ridge is the same as that used for the SOA, with a length of 20µm. Figure 3.4 exhibits the SEM image of the SOA-PIN before the metallization.

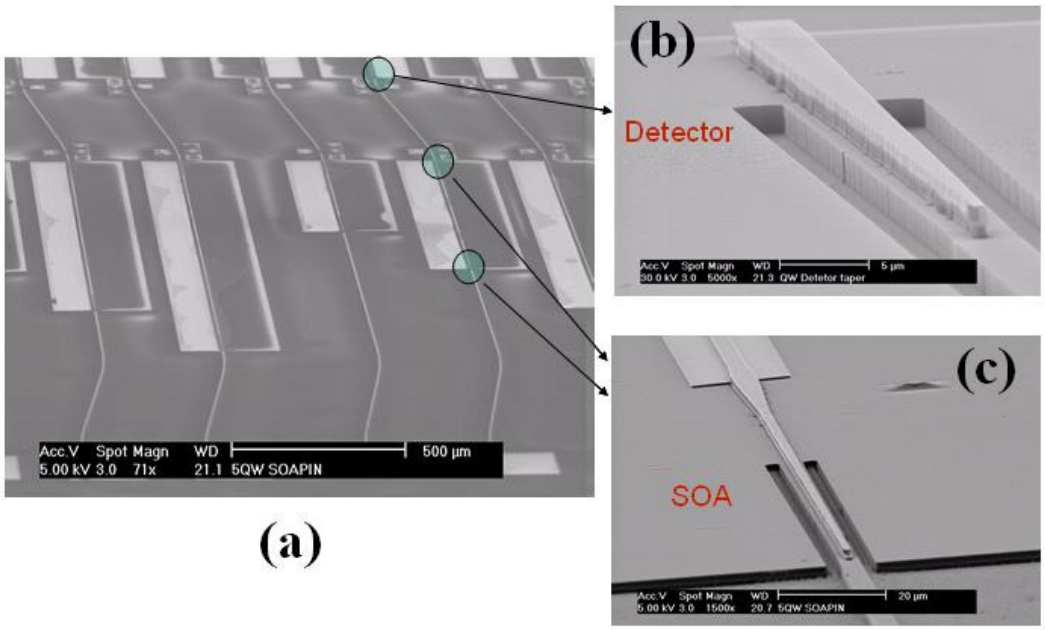

Fig. 3.4 *SEM image of the SOA-PIN before metallization: (a) overview of SOA-PIN (b) individual detector (c) individual SOA*

3.3 Characterization of the integrated optical receiver

The device is mounted p-side up on a copper heat sink held at 13^0C. A lensed fiber is used to launch the light into the dilute waveguide. Since the QWs are compressively strained, only the transverse-electric (TE) mode is expected to experience gain and detection.

The DC photocurrent of the QW photodetector is measured using an Agilent 4556C parameter analyzer with a Santec TSL-210 tunable laser. Figure 3.5 shows the dependence of the DC external responsivity of the photodetector on wavelength (λ) at –5 V bias. At λ=1550nm, a peak external responsivity of 0.45±0.05 A/W (without antireflection coating) is achieved. This corresponds to nearly 90% internal quantum efficiency. Between λ=1530nm and 1570nm, the responsivity varies by 1.5 dB. Outside of this wavelength window, the decrease in responsivity is due to the characteristically narrow QW absorption spectrum [9], and the wavelength dependent transfer efficiency of the adiabatic taper, described at Ref [30] at Chapter 1.

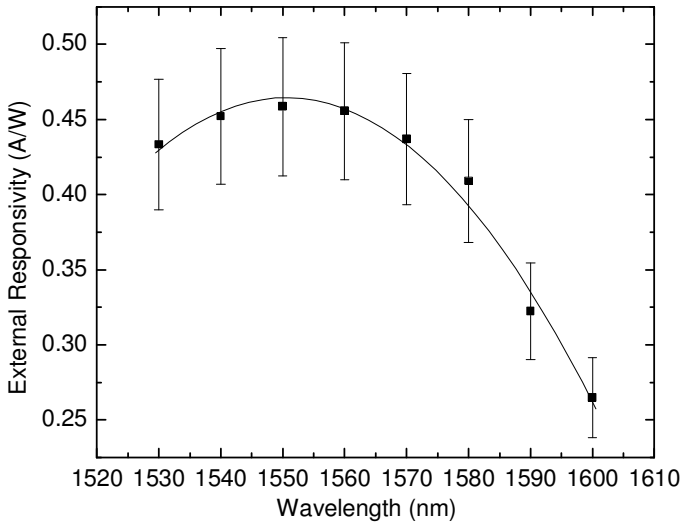

Fig. 3.5 *Fiber-to-detector responsivity of the quantum well tapered photodetector at –5V bias. The peak responsivity is 0.45±0.05 A/W at λ=1550nm. The non-uniformity is within 1.5dB between λ=1530nm and λ=1570nm.*

For the photodetector, the speed is also as important as its responsivity. Figure 3.6 presents the AC frequency response of the detector at λ=1550nm. The data reveals a 3-dB optical bandwidth of 11±1 GHz. The small signal S_{11} scattering parameter of the photodiode measured using an HP8703A network analyzer suggests a total capacitance of

C=225fF, and a series resistance of R=8.5Ω, corresponding to an RC time constant of 13 ps after considering the transmission line load of 50Ω. Since the 3-dB bandwidth of the photodiode is determined by the carrier transit time and the RC time constant, the measured S_{11} scattering parameter suggests that the speed of the tapered photodiode is limited primarily by the RC time constant, dominated by the parasitic capacitance.

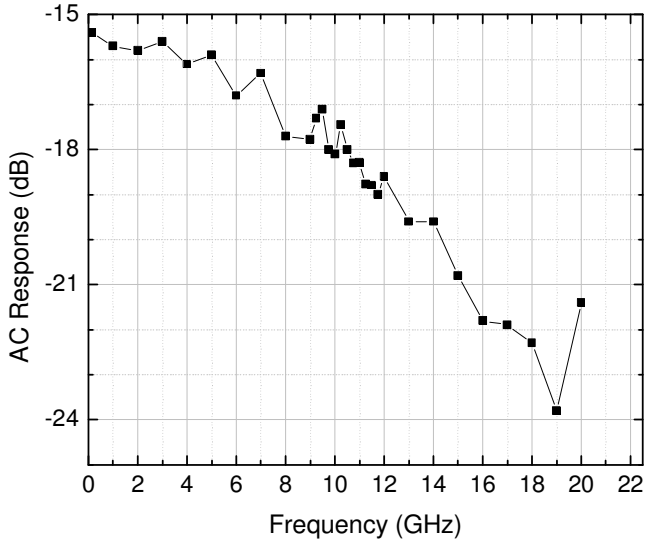

Fig. 3.6 *Frequency response of the quantum well tapered photodetector at –5V bias. The 3dB bandwidth is 11±1 GHz. Compare this result to the S_{11} scattering parameter, the 3dB bandwidth of the tapered photodiode is limited by the RC time constant.*

Figure 3.7 shows the external responsivity of the integrated optical receiver at various SOA currents. The external responsivity variation is less than 1.5-dB between λ=1530nm and 1555nm, shown in Fig. 3.8, and a peak external responsivity of 8.2±0.4 A/W is achieved at a drive current of 115mA and λ=1540nm. Compared to a single detector, the wavelength tolerance of SOP-PIN is also dominated by the amplified spontaneous emission (ASE) spectrum of the SOA, shown in Fig. 3.9. The responsivity of the tapered photodetector is linear up to an input power of 7mW, with a fiber-to-

detector gain of 8.8±0.2 dB. At the highest driving current, the gain is probably limited by Joule heating of the SOA [10]. Furthermore, imperfect BCB planarization will increase contact resisitance and therefore lowers the current injection efficiency of the SOA.

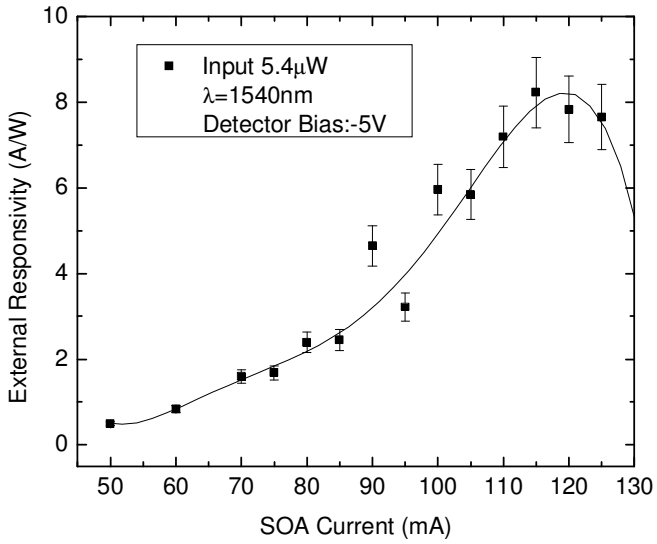

Fig. 3.7 *External responsivity as a function of SOA drive current.*

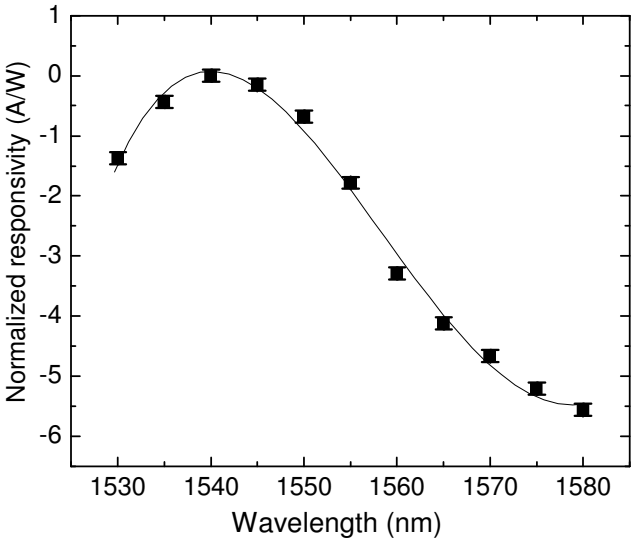

Fig. 3.8 *Normalized external responsivity as a function of wavelength*

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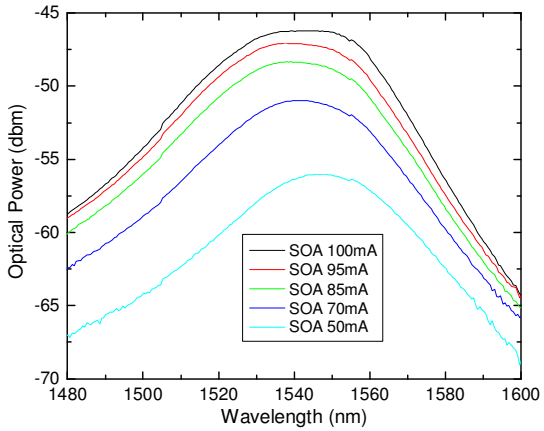

Fig. 3.9 *ASE spectra of the SOA as a function of pump current. The peak shifts to lower wavelengths indicating dominance of bandfilling over heating till heating.*

Figure 3.10 shows the frequency response of the integrated optical receiver. The responsivity increases with increasing SOA current (and hence gain). The 3 dB bandwidth is 11±1 GHz, also limited by the RC bandwidth of the tapered photodetector. Considering the fiber-to-SOA coupling loss, scattering loss, and free carrier absorption from the taper and passive waveguide, an internal SOA gain of 13.8±0.2 dB is inferred, from which we estimate a total receiver internal gain-bandwidth product of 265±35 GHz.

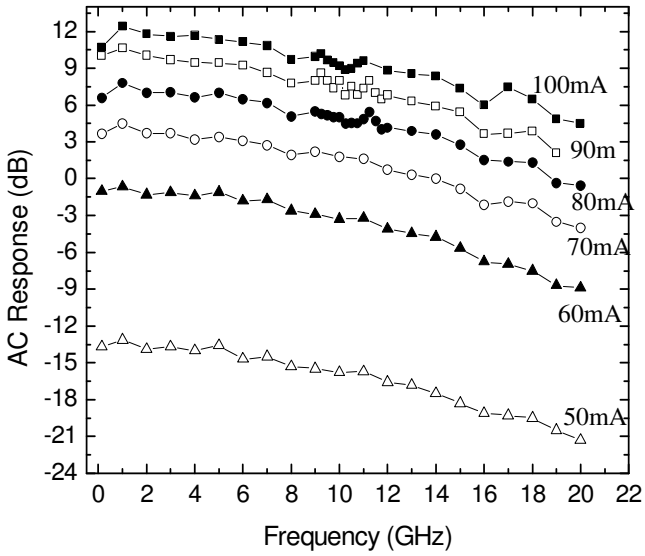

Fig. 3.10 *RF response Vs. frequency for different SOA drive currents*

The sensitivity of the integrated optical receiver can be estimated by considering the signal-spontaneous and the spontaneous-spontaneous beat noise from the SOA when it is biased at the maximum current, 115 mA [10]. The spontaneous emission factor, N_{sp}, and the spontaneous emission power, i_{sp}, are estimated by the measured photocurrent purely excited by the ASE of the SOA. Here, we assume that the extinction ratio of a typical input WDM signal, provided by a commercial semiconductor laser, is 0.05. By considering the fiber coupling loss of 4 dB, measured responsivity of the p-i-n detector, the internal SOA gain of 14 dB, and the optical bandwidth of 30nm, the maximum sensitivity, shown in Fig 3.11, is calculated to be -25dBm. Fig. 3.11 also indicates that the sensitivity of SOA-PIN receiver exhibits a >9dB improvement compared to a stand-alone p-i-n tapered photodiode.

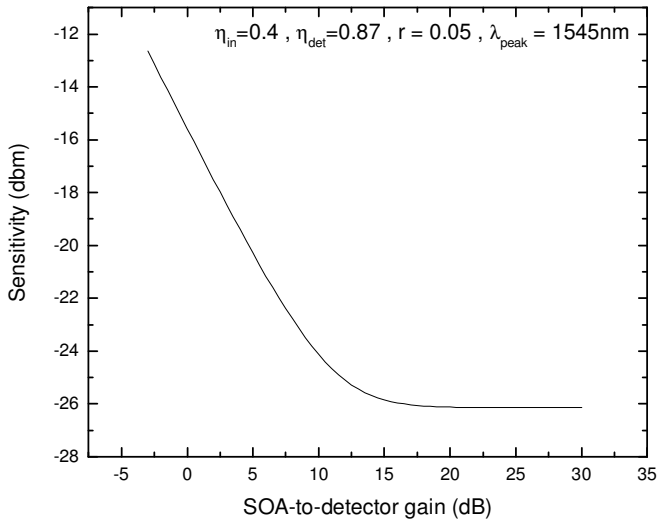

Fig. 3.11 *Calculated sensitivity of the SOP-PIN receiver*

Table 3.1 compares the principle features of this optical receiver with other comparable devices previously reported in the literature. All integrated receivers, except that in [7], use the same material for both amplification and detection. In [5], several selective area growth steps are required for integration while [4] needs only one step of

material regrowth. The work done by Xia [7] is regrowth free, but requires a complex fabrication process, and also suffers from the loss in the unpumped active region when the light is transferring from the active guide to the coupling guide. In contrast, the circuit demonstrated here provides a method for photonic integration without material regrowth and complex fabrication steps. All of the reported receivers have nearly unity of internal quantum efficiency. Neverthless, the low optical gain provided by the SOA in this work leads to the overall inferior external responsivity which can be mitigate by further optimizing material growth and the ohmic contact.

3.4 Summary

In this chapter, we have demonstrated a monolithically integrated optical receiver without material regrowth and complex fabrication steps. The receiver exhibits a peak external responsivity of 8.2±0.4 A/W, and a 3 dB bandwidth of 11±1 GHz, corresponding to an internal gain-bandwidth product of 265±35 GHz. The success of this work suggests that sharing of the same active material for both light generation and detection with ATG technology provide a powerful approach for integrating multiple active components on the ROADM circuit.

Table 3.1: Comparison of different integrated optical receivers

	This work	Tauke-Pedretti, et al. [4]	Mason, et al. [5]	Xia, et.al. [7]
Material system for gain/detection	1% compressive InGaAsP 5QWs	7QW	-0.4% tensile bulk InGaAs	1% compressive InGaAsP 5QWs
SOA configuration	1mm long 3.5μm wide	600μm long flared SOA	600μm long 1.8μm wide	2.4mm long 3.2μm wide
photodiode configuration	150 μm long taper 20μm long ridge	50μm long Tapered p-i-n	80μm long 1.8μm wide	25μm long 7μm wide
Peak responsivity (A/W)	8.23±0.4 (A/W) w/o ARC[(a)]	25 (A/W) w/ ARC[(b)]	15.9[(b)] (A/W)	5.5[(c)] (A/W) w/ ARC
Peak SOA gain (dB)	8.8 @ 115mA	14 @ 250mA	14 @ 65mA	9.5 @ 220mA
3 dB bandwidth (GHz)	11±1	15	40	36

(a) ARC=Anti-reflection coating

(b) Assume load of the photodiode is 50Ω

(c) Inferred from the fiber-to-SOA coupling loss in ref [5]

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Chapter 4

Implementation of the InP-based ROADM

4.1 Introduction

The discussion at Chapter 1 has illustrated various existing ROADM technologies, which require sophisticated packaging and are limited to the scope of passive components. In this chapter, we combine the passive and active components discussed in Chapter 2 and 3 to demonstrate an InP-based monolithically-integrated reconfigurable optical add-drop multiplexer. This ROADM circuit consists of an array waveguide grating, a semiconductor optical amplifier, four 2x2 Mach-Zehnder optical switches, and four PIN photodetectors. The total chip size is 10mm x 6mm, and each of the components in the circuit exhibited performance similar to that achieved in a discrete form. The add/drop functionality of the chip is demonstrated via the routing of a signal from the add port to the drop/output port.

4.2 Design and fabrication of the ROADM circuit

As described at chapter 1, a typical ROADM circuit requires one DEMUX to isolate the incoming WDM channels, and another MUX to combine individual processed WDM channels. To minimize the chip area and avoid the fabrication mismatch between two different AWGs, we adopt the loop-back structure to have the MUX and DEMUX share the same AWG [1]. Figure 4.1 is the basic building block of the ROADM circuit. Under the loop-back configuration, a single 5 x 5 AWG reserves one common input and output waveguide while the remaining four output waveguides connect with the

corresponding input waveguides at the other side. The add port and drop port of the ROADM circuit is composed of an array of optical switches and photo-detectors, respectively. Due to reversibility of the AWG, the processed WDM channels will be focused on the common output waveguide, which is also the output port of the ROADM.

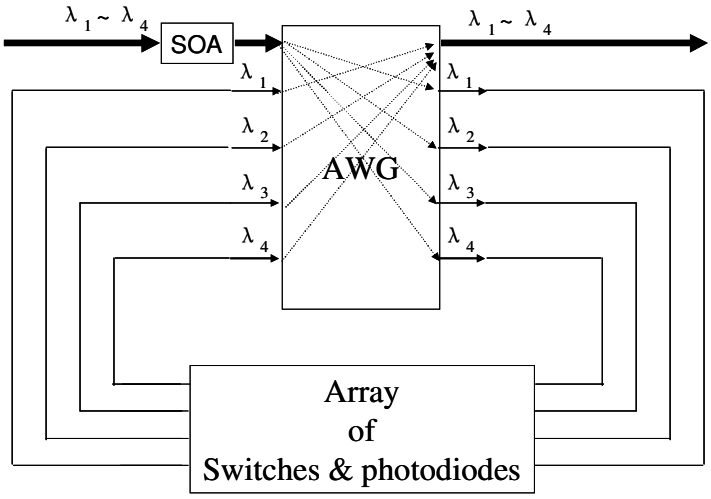

Fig. 4.1 *Schematic of 4-channel ROADM based on AWG loop-back architecture (The add port is not shown here.)*

Figure 4.2 shows the layout of the monolithically integrated 4-channel ROADM [2]. It consists of two 5x5 array waveguide gratings (AWG) followed by four 2x2 Mach-Zehnder interferometer (MZI) optical switches [3]. The PIN detectors are located at the drop ports. Both the PIN detectors and SOA use the same compressively strained quantum wells for light absorption and gain generation [4]. The dimension of the dilute waveguide, SOA, PIN detectors, and the adiabatic tapers for SOA and PIN detectors are the same as in Chapter 4 except that the length of the SOA ridge is 1.5mm. The 3-dB multimode interference (MMI) coupler used for the MZI optical switches is 570μm long by 11.5μm wide. The length of the metal contact of the optical switches is 300 μ m. The total chip dimension is 10mm by 6mm.

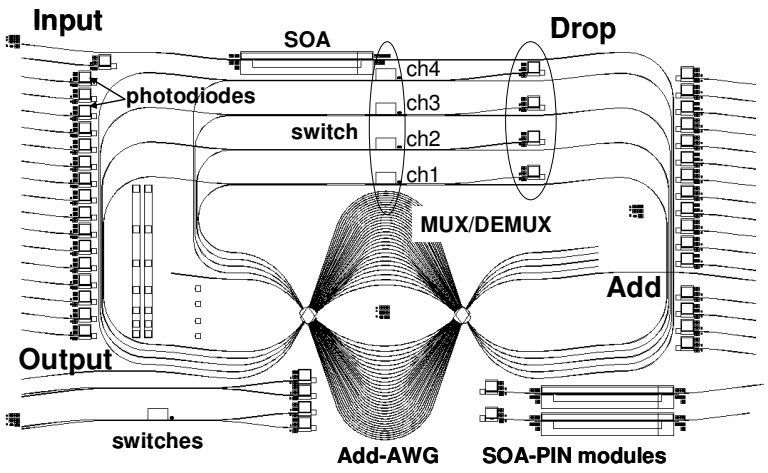

Fig. 4.2 *The mask layout of the 4-channel ROADM*

The WDM signal input from the fiber is coupled to the input port of the ROADM, and is amplified by the SOA. The light propagating in the waveguide is demultiplexed by the AWG, and routed to the corresponding optical switches. The current-driven optical switches direct the signal either to the drop ports and detected, or to the multiplexer. Since the AWG applies loopback architecture [1], the multiplexed signals propagate once again through the AWG, combined, and then sent to the output port. A new wavelength channel can be added by coupling the light to the add-AWG. The add-AWG routes the signal to the corresponding waveguide, thereby adding it to the other WDM channels.

The epitaxial structure of the ROADM is grown by gas source molecular beam epitaxy on a (100) Zn-doped InP substrate. The composition and thickness of the passive waveguide, the gain/detection material, and the contact layer are the same as in [4]. To accommodate the active devices and the current-driven optical switches on the same chip, the doping of the wafer is chosen to be p-i-n-i-p. To minimize free carrier absorption in the waveguide, the passive waveguide is undoped, except for the top Si-doped ($5x10^{17}cm^{-}$

[3]) InP layer of thickness 0.45μm, which serves as the n-contact layer for the optical switches, PIN detectors, and SOA. Detailed epilayer structures are provided in Table 4.1.

Table 4.1. Layer structure of the ROADM

Material	Thickness	Doping	Function	
P-InP	~120μm	Zn	Substrate	
InP	0.75μm	Undoped	Buffer layer	
InGaAsP (Eg=1.03eV)	0.165μm	Undoped	Fiber guide	
InP	0.45μm	Undoped		
InGaAsP (Eg=1.03eV)	0.18μm	Undoped		
InP	0.45μm	Undoped		
InGaAsP (Eg=1.03eV)	0.195μm	Undoped		
InP	0.15μm	Undoped		
InP	0.45μm	Si $5x10^{17}cm^{-3}$		
InGaAsP (Eg=1.03eV)	0.12μm	Undoped	SCH layer	
InGaAsP (Eg=0.78eV)	0.0135μm	Undoped	1% compressive quantum well	x 5
InGaAsP (Eg=1.03eV)	0.023μm	Undoped	Barrier	
InGaAsP (Eg=1.03eV)	0.097μm	Undoped	SCH layer	
InP	0.15μm	Undoped	Separation layer	
InGaAsP (Eg=1.03eV)	0.03μm	Be $10^{17}cm^{-3}$	Etchstop layer	
InP	1μm	Ramped, Be $10^{17}cm^{-3}$ to $10^{18}cm^{-3}$	Cladding layer	
InGaAsP (Eg=0.75ev)	0.2μm	Ramped, Be $10^{18}cm^{-3}$ to $2x10^{18}cm^{-3}$	Contact layer	

Fabrication of the ROADM follows the procedures reported previously [5], with the p-metal consisting of Ti/Pt/Au annealed at 425 ^{o}C for 30 s. The n-metal for the SOA and the PIN detectors is Ge/Au/Ni/Au, while Ti/Au is used for the n-metal of the optical switches. Both n-metals are annealed at 360 ^{o}C for 90 s. To minimize the dark current, the wet etchant (H_2SO_4: H_2O_2: H_20 = 1:1:10) is used to polish the sidewall of the detectors after reactive ion etching. Figure 4.3 is the SEM image of the entire circuit after the fabrication.

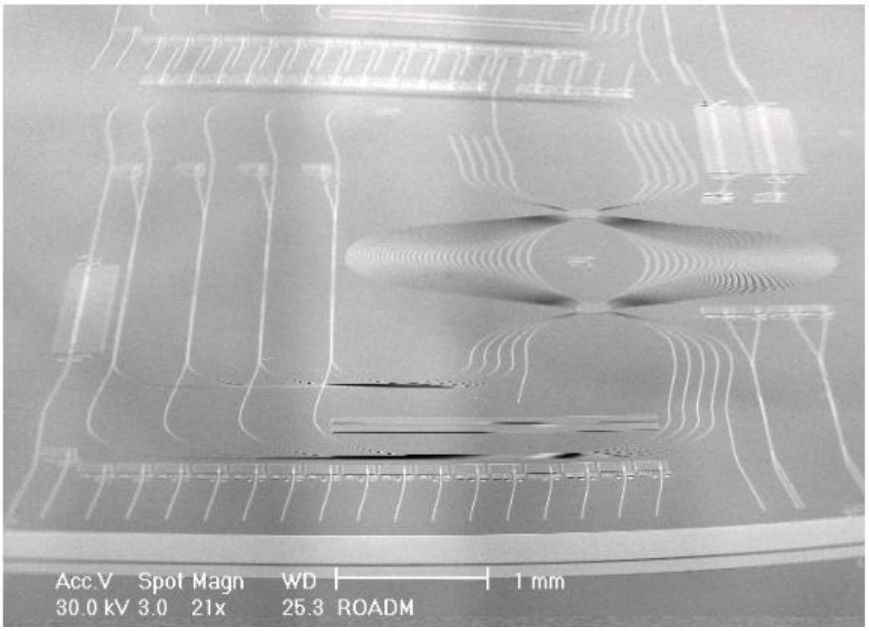

Fig. 4.3 *The SEM image of the 4-channel ROADM*

4.3 Characterization of the individual optical components in the ROADM

The chip was mounted on a copper heat sink, and lensed fibers were used to launch and collect the light. Measurement details are identical to those described in Chapter 3. Since the gain/detection regions are compressive QWs, the circuit is only sensitive to transverse-electric (TE) field modes.

To allow for characterization of the individual components, a number of discrete QW photodiodes, SOA-PIN modules, and optical switches are embedded in the chip. Typically, the dark current of discrete, 300μm^2 photodiodes is < 1nA at –5V bias voltage. As shown in Fig 4.4, the peak external responsivity of the individual detector without antireflection coating is (0.29±0.05) A/W at λ=1540nm. Since the variation of the responsivity is within 1dB between λ=1530nm and λ=1570nm, each channel of the drop port employs the same adiabatic taper geometry.

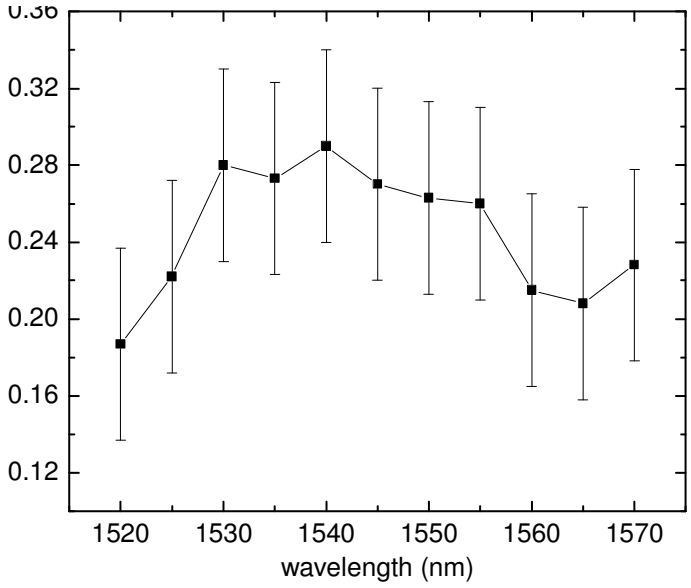

Fig. 4.4 *External responsivity of the individual quantum well photodiode versus input wavelength.*

Figure 4.5 shows the external responsivity of the SOA-PIN module at various SOA currents. A peak responsivity of (12.5±0.5) A/W is achieved at a current of 150mA at λ=1570nm. Taking into account the responsivity of the photodiode, the gain provided by the SOA is 16dB. At the highest driving current, the gain is limited by Joule heating of the SOA. The frequency response of the quantum well photodiodes and the SOA-PIN

module is expected to be (11±1) GHz, since the gain/detection material and the device geometry are identical to that described at Chapter 3. Compared to the SOA-PIN device demonstrated in Chapter 3, this SOA exhibits lower optical gain per unit length because there is only 0.45 μm of n-InP n-contact layer. Also, as indicated in Fig 4.6, the active waveguide at the taper region cannot provide high gain because the current injection into the taper region is limited due to high resistance from the narrow taper structure.

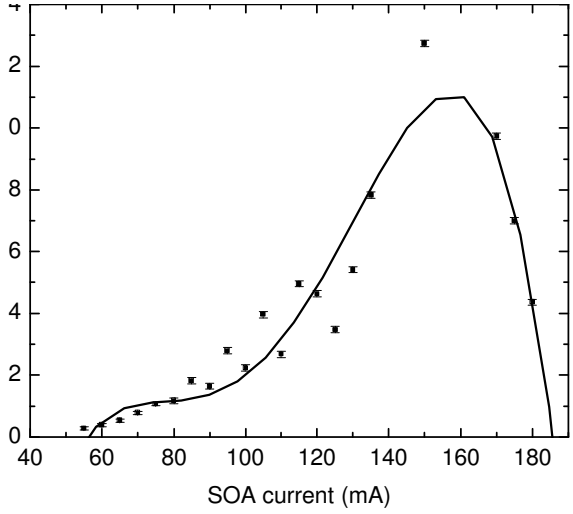

Fig. 4.5 *External responsivity of the individual SOA-PIN module at λ=1570nm with various drive current.*

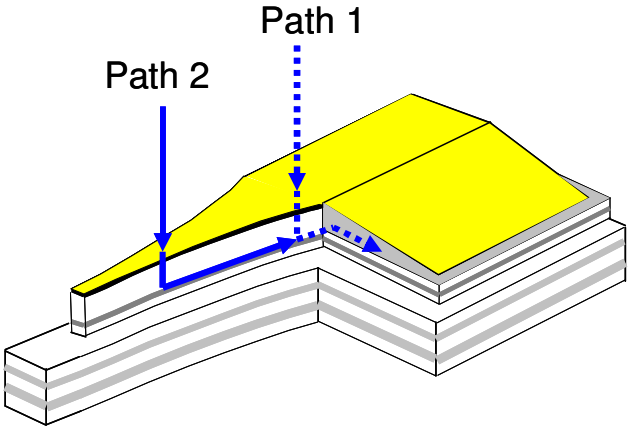

Fig. 4.6 *Current injection path of the SOA-PIN in the ROADM circuit. Path 2 is more resistive than path 1 due to the narrow taper. Therefore, the active waveguide at the taper region will provide less gain than the one at the shallow ridge region.*

Figure 4.7 shows of the light output of the optical switches and the fitting curve following the procedure of the calculation in Chapter 2. Due to the insufficient undercut of the reactive ion etching, the MMI is 0.3μm wider than the intended design, leading to an on/off contrast ratio of 18±1 dB. Accounting for coupling loss from the fiber to the waveguide, the insertion loss of the optical switch is approximately 1.5dB. Heating from non-optimized n-metal contacts slightly reduces the refractive index modulation of the switches, and thus affects the contrast ratio at high currents. Due to the nature of MMI coupler, the switch is wavelength insensitive over the range of wavelengths channels used in this ROADM.

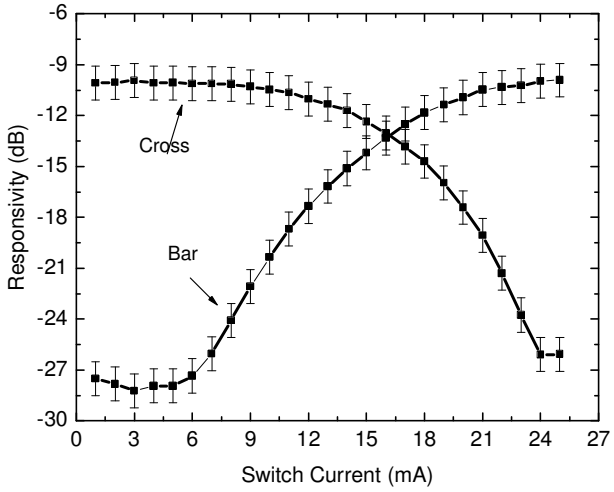

Fig. 4.7 *Contrast ratio of the individual optical switch at various drive currents.*

The five-channel multiplexer/demultiplexer AWG consists of 30 array-waveguides, at a channel spacing 2nm, a free spectral range 10nm, and a minimum radius of curvature of 700μm. As shown in Fig 4.8, the insertion loss and crosstalk of the AWG are12±2dB and –15±2dB, respectively. Lack of an antireflection coating, limited number of array waveguide arms at the star coupler, and the propagation loss due to the n-contact layer may result in the higher insertion loss than the gain of the integrated SOA. The

crosstalk can be further improved by increasing the gap of receiving waveguide at the image plane of the star coupler [6].

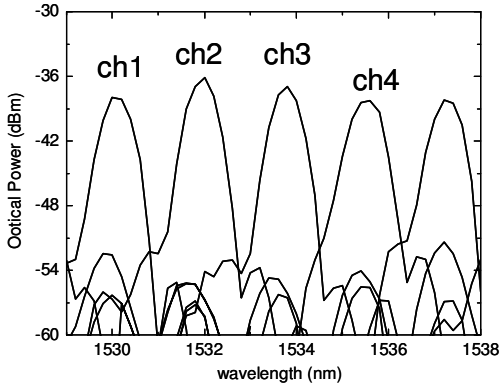

Fig. 4.8 *Spectrum of the individual 5x5 AWG in ROADM*

4.4 Characterization of the ROADM circuit

The add/drop functionality of the ROADM was first tested by launching the light into the add port. As shown in Figure 4.9, when the switches are in the OFF state, the light at the add port propagates directly to the drop port where it is coupled to the integrated photodiodes.

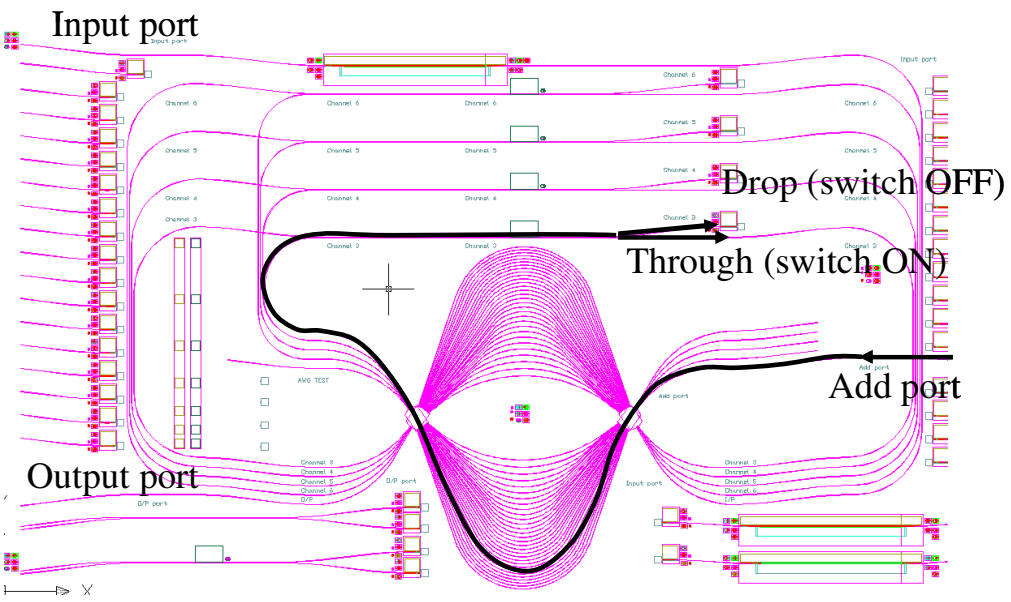

Fig. 4.9 *The data flow used to test the add/drop function of the ROADM circuit*

Figure 4.10 (a) is the overall photocurrent spectrum at the drop port following the data flow from the add port to the drop port. The behavior of this photocurrent spectrum is primarily determined by the characteristics of the AWG, and therefore has a crosstalk of -15.5±1.5dB and non-uniformity of 1 dB. On the other hand, when turning the switch on, the signal is directed to the multiplexer, resulting in the photocurrent drop at the corresponding photodiode. Figure 4.10 (b) shows that each individual channel drops by 20±1 dB by sweeping the input wavelength, and this matches the contrast ratio of the optical switches on-chip.

The spectrum at the output port is primarily determined by the behavior of the AWG. Figure 4.11 shows the spectrum of channel 4 from the add port to the output port with the switch in the ON and OFF modes. The channel dropping extinction ratio is 20±1dB, which is consistent with the measurement shown in Fig 4.10 (b). The adjacent ripples near the peak arise from the crosstalk of the AWG.

Finally, the through function of the ROADM circuit was tested by measuring the wavelength dependence of the light intensity at the output port. Due to the loop-back architecture, channel 1 through channel 4 will pass AWG twice while the fifth AWG channel, λ_5, will pass AWG only once and directly reach the output port. Figure 4.12 is the spectrum at the output port by doing the wavelength sweep at the input port. Between the periods of λ_5, only spurious signals can be seen, which is associated with signal degradation due to the insertion loss of the ROADM that can not compensate the interference from the AWG crosstalk. Since the InP-based AWG can reach the insertion loss as low as 2.5 dB and the crosstalk as high as 30 dB [7], the issue of spurious readout can be reconciled by further optimizing the design and fabrication of the AWG device.

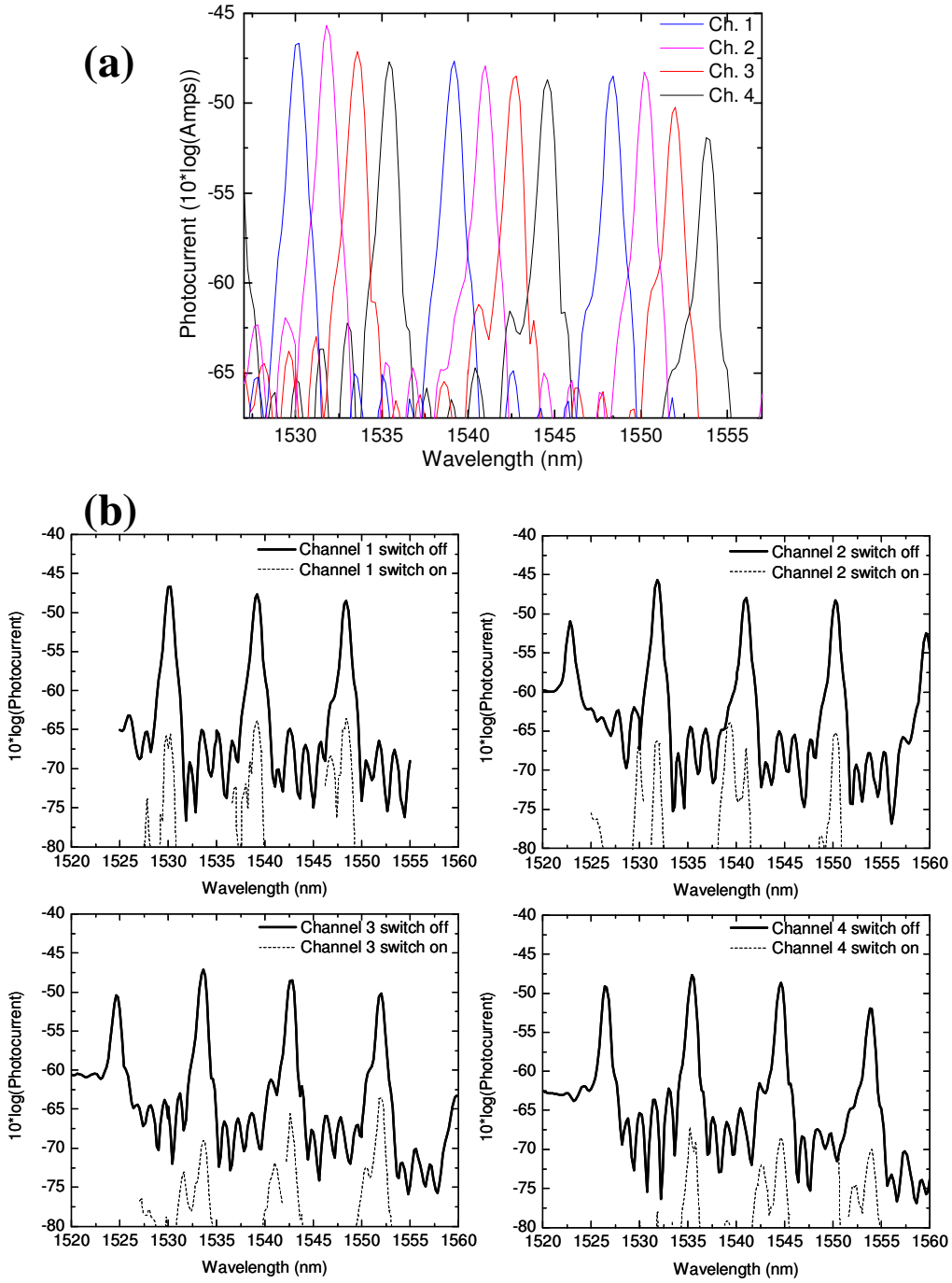

Fig. 4.10 *(a) Overall photocurrent spectrum at the drop port with all of the switch at the OFF-state. (b) The individual photocurrent spectrum when the corresponding switch is in both the ON (to through port) and OFF (to drop port) state*

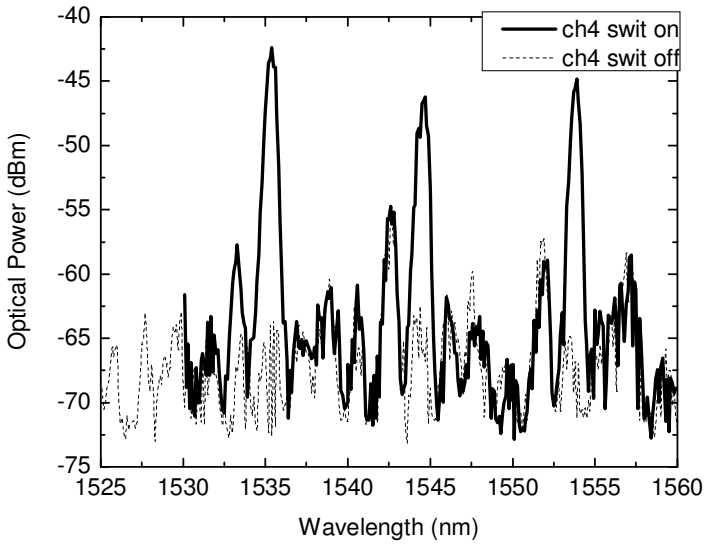

Fig. 4.11 *Optical spectrum of channel 4 at the output port with the switch in the ON and OFF state.*

4.5 Summary

In this chapter, we have demonstrated a monolithically integrated ROADM based on ATG technology. The integrated SOA and photodiodes provide both light amplification and detection on a single chip. Full add/drop functionality has been exhibited. From Chapter 2 and 3, the speed of individual optical switch and photodetector is 10ns and 0.1ns, respectively. Each will determine the speed of reconfiguration and channel-download of this ROADM, respectively. Nevertheless, due to the thinner n-contact layer in this ROADM than the one at Ch.2 and Ch.3, the series resistance of both integrated switch and photodetector will be higher and thus the larger RC time. On the other hand, the most important challenge is that the high insertion loss and crosstalk of AWG limit the ability of the through function of the ROADM. Nevertheless, by combining this work with the past success of purely passive InP-based ROADM [7], it suggests that the InP-based monolithic integrated ROADM still has great potential for future low cost WDM networks.

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Chapter 5

Enhancement mode MOSFET with high-κ gate dielectric on InP substrate

5.1 Introduction

The successful demonstration of functionality of add/drop of ROADM at previous chapters fully proves the feasibility to achieve complex integrated lightwave system via InP-based material and ATG technology. On the other hand, to further reduce packaging complexity, production cost, and enhance reliability [1], the ultimate goal of the integration is to have optoelectronic integrated circuits which combine both of photonic and high speed electronics on a single substrate. Due to relative high conduction band discontinuity, electron mobility, and peak drift velocity than GaAs and Si, InP-based III-V semiconductors are promising materials system for high speed electronic devices [2]. Thus, due to their combined strengths for optoelectronics and electronics, InP-based compound semiconductors are most likely to ensure the integration of photonic devices and electronic circuits. In this chapter, we demonstrate a prototype of individual InP-based metal-oxide-semiconductor field-effect transistor (MOSFET) device for future integration of high speed electronics with photonic elements [3]. This work was performed in collaboration with IBM T.J. Wastson Research Center.

5.2 Device design and fabrication

In general, MOSFET is a surface-channel device in which the carriers flow at the interface between semiconductor and gate dielectric. However, due to surface Fermi-level pinning of III-V materials, surface-channel III-V MOSFETs typically contain an ultra-high density of interface states (D_{it}) which reduce the carrier mobility and ON/OFF current ratio [4]. We utilize a buried-channel MOSFET to separate the carriers from the surface D_{it} [5-7].

The detail device structure is shown in Fig. 5.1. The epitaxial layer is grown by GSMBE on a (100) Fe-doped, semi-insulating InP substrate. The MOSFET channel is a 10 nm undoped In0.7Ga0.3As strained QW confined with a 300 nm undoped $In_{0.52}Al_{0.48}As$ buffer layer, and a 10 nm undoped $In_{0.52}Al_{0.48}As$ top barrier layer. The final cap layer is a 25 nm In0.53Ga0.47As (Si-doped, $1x10^{19}cm^{-3}$) cap layer. To characterize D_{it}, another sample consisting of a single n-type $In_{0.52}Al_{0.48}As$ bulk layer is also grown on n-type InP substrate and subsequent fabricated into MOS capacitors. The detailed growth condition is described at ref [10] of Chapter 2.

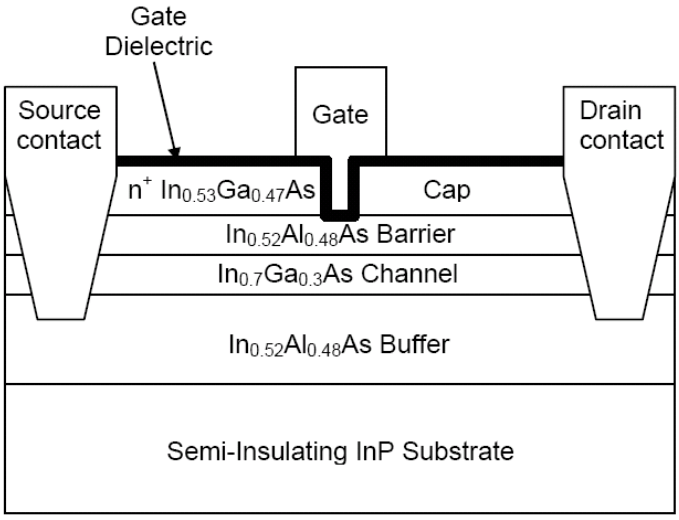

Fig. 5.1 *Device structure of the InGaAs buried channel MOSFET.*

The fabrication starts from defining gate recess area by either optical lithography for long channel MOSFET, or electron-beam lithography for short-channel device, followed by selective wet-etching of top n^+-InGaAs cap layer. After the gate recess, the sample is dipped with dilute HF and capped with thin amorphous silicon interlayer by PECVD, before the gate dielectric is deposited. After selectively etching the high-κ dielectric, the source/drain metal contact, consisting annealed Au/Ge/Ni, and the gate metal contact are then defined by optical lithography and lift-off. The short-channel device fabrication included an additional mesa isolation step before the gate lithography. The resulting long channel device has gate length of 5 μm with Al gate contact and Al_2O_3 dielectric, while short channel device has gate length of 260nm with Al or Pt gate contact and HfO_2 dielectric. The fabrication of MOS capacitor starts from the same surface pretreatment as that of MOSFET device, followed by 6nm of Al_2O_3 dielectric deposited by atomic layer deposition (ALD), and 100nm of Al front/back contact.

5.3 Characterization of the long/short channel MOSFET

The current-voltage characteristics of the MOSFET and the gate capacitance-voltage (C-V) of MOS were measured using an HP 4156A parameter analyzer and HP 4284A LCR meter, respectively. Figure 5.2 (a) presents the C-V data of the n-InAlAs MOS capacitor as a function of measurement frequency. Based on the equivalent circuit of MOS capacitor [8], the capacitance associated with D_{it} is in parallel with semiconductor depletion capacitance. Hence, the frequency behavior of D_{it} causes the frequency dispersion of C-V curve. As shown at Fig 5.2 (b), the distribution of Dit, induced from Fig 5.2(a) by high-low frequency method [9], is basically U-shape with

minimum of $4x10^{12}/cm^2eV$ near the mid-gap. Such a high D_{it} level is likely responsible for the non-ideal subthreshold slope of subsequent MOSFET devices in this work.

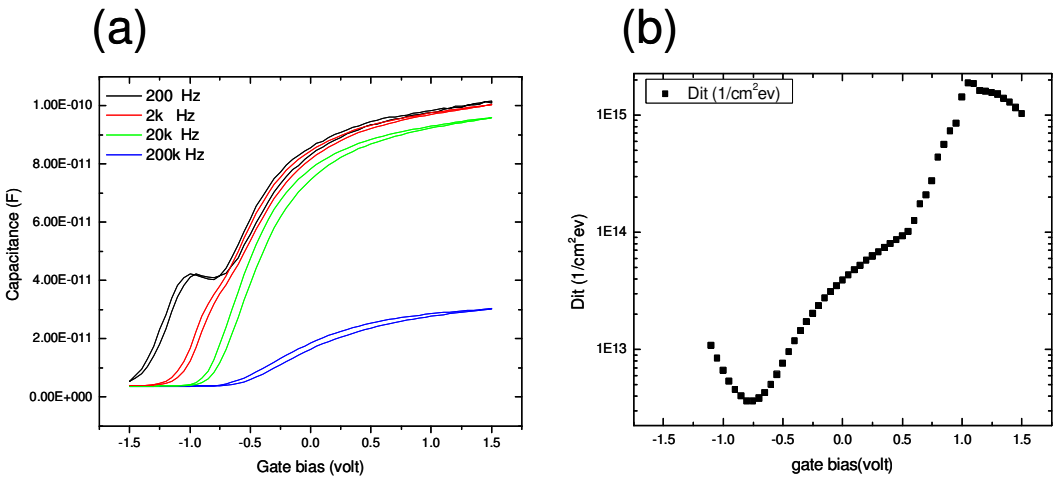

Fig. 5.2 *(a) C-V (b) D_{it} distribution of n-InAlAs/n-InP MOS capacitor measured under dark environment.*

The plot in Fig. 5.3 (a) shows the sub-threshold and gate leakage characteristics of the long channel MOSFET. The peak extrinsic transconductance is 42mS/mm when V_{gs} = 0.95 V and V_{ds} = 2 V. By doing linear extrapolation from the peak extrinsic transconductance at V_{ds} = 50 mV, the threshold voltage is estimated to be about 0.25 V, which indicates that this long-channel device is an enhancement mode MOSFET. The drain current on-off ratio is ~ 10^4, and sub-threshold slope is around 150 mV/decade. The gate leakage current density of the same device, also shown in Fig. 5.3 (a), is at least orders of magnitude lower than its HEMT counterpart [7]. Figure 5.3 (b) is the gate C-V curves of the buried-long-channel MOSFET. The mid-gap D_{it} obtained from conductance method for these devices is in the high $10^{12}/cm^2eV$ range, which is consistent with large frequency dispersion of C-V curve at the accumulation region when the gate has positive forward bias.

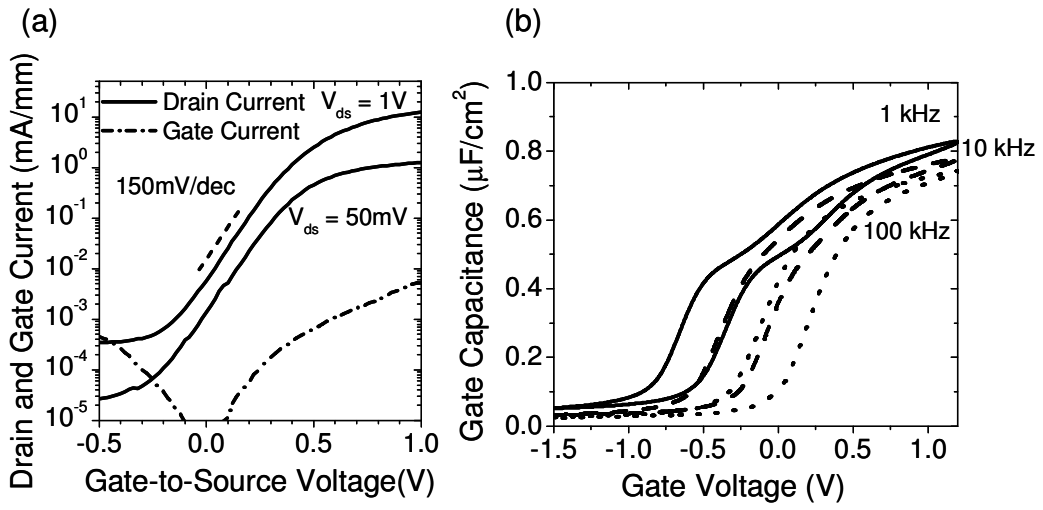

Fig. 5.3 *(a) Sub-threshold and gate leakage I-V and (b) frequency-dependent C-V curve of the long-channel MOSFET.*

Figure 5.4 (a) is the sub-threshold of short channel MOSFETs with either Pt or Al gate metal. Following the same procedure from Fig 5.3(a), the threshold voltages are 0.5 V and -0.2 V for Pt and Al gate metal, respectively. Due to surface Fermi-level pinning (high D_{it}), the difference between both threshold voltages is less than the work function differences between gate metals. The enhancement-mode device (V_t = 0.5 V) has drain current on-off ratio of ~ 10^3, and sub-threshold slope of ~ 200 mV/dec. The DC output characteristics of the short-channel enhancement mode MOSFETs, shown at Fig 5.4(b), exhibits good saturation and pinch off characteristic with a significant series resistance. This series resistance is primarily due to the large gate-to-drain metal or gate-to-source metal distance, which is 2.4 μm. As shown in Fig. 5.5, a similar device with smaller gate-to-drain metal or gate-to-source metal distance (0.4 μm) shows three times higher drive current than Fig. 5.4(a), which exhibits extrinsic maximum transconductance of 157 mS/mm at V_{ds} = 0.6 V and V_{gs} = 0.65 V. Comparing to its HEMTS counterpart, both DC characteristics of MOSFET can be further improved by optimizing ohmic contact [7].

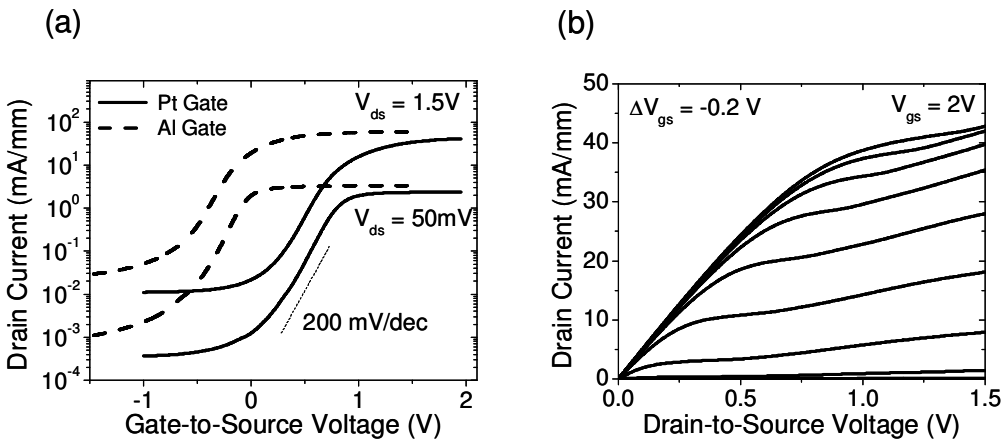

Fig. 5.4 *(a) Sub-threshold and gate leakage I-V , and (b) DC output characteristics*

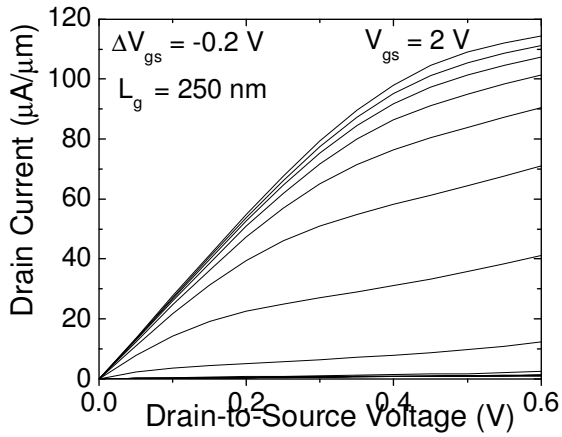

Fig. 5.5 *DC output characteristics of the short-channel MOSFET with 0.4 μm separation between gate and source/drain with various gate bias.*

From the above characterization, it is found that the typical D_{it} of III-V transistor is always above $10^{12}/cm^2eV$ even after surface passivation by dilute HF dip. Nevertheless, the demonstration of enhancement mode MOSFET and tuning of threshold voltage via various different gate metals in this work indicates that the buried channel structure can partially reconcile the issue of high D_{it}. On the other hand, the final drain current is still limited by the high series resistance. To mitigate this issue, further optimization of the source/drain ohmic contact and the adoption the scheme of self-aligned source/drain

contact, which gives ~zero separation between source/drain metal contact to the channel, are needed.

5.4 Summary

In this work, in collaboration with IBM T.J. Watson Research Center, we demonstrated long- and short-channel, enhancement-mode, strained InGaAs MOSFETs with high-κ gate dielectrics on InP substrate. To mitigate the influence from the high interface state, we adopt the structure of buried channel to isolate the inversion carriers from the surface. Various gate metals have been chosen to ensure the MOSFET operating at the enhancement mode. For the time being, this work demonstrates the state-of-the-art III-V MOSFET which high transconductance and drive current. The peak transconductance is 42 mS/mm and 157 mS/mm for long- and short- channel MOSFET, respectively while its sub-threshold slope is between 150 mV/decade and 200 mV/decade. The non-ideal sub-threshold slope is due to high D_{it} at high-κ dielectric and InAlAs interface. The simple layer structure of MOSFET and the successful demonstration of this work illustrate the feasibility of having high speed electronics integrated with photonic integrated circuit on the single InP substrate.

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Chapter 6

Overview of solar cell technologies

The development of solar cells has been expedited in the last decade due to the increased price of fossil fuels. The best bulk III-V tandem cell has demonstrated the efficiency of 32% under 1 sun illumination [1] while First Solar, Inc has declared that the production cost of CdTe thin-film photovoltaic (PV) module is now below $1.0 per Watt. Nevertheless, the development of III-V thin-film type solar cells which have high efficiency is still in its infancy. This part of the thesis (Chapter 6-9) describes the feasibility of III-V thin-film solar cells based on InP Schottky type thin-film solar cell bonded onto a plastic sheet for achieving low cost. In this chapter, we will overview the working principles and some general characterization techniques for solar cells. Then, we will do a cost analysis of thin-film type solar cells based on crystalline GaAs. The details of the device fabrication and characterization will be discussed in succeeding chapters.

6.1 Solar cell principles

A solar cell is either a Schottky junction or p-n junction operating in the absence of an external applied voltage. When illuminated with sunlight, photons with energy larger than the bangap are absorbed by the semiconductor. This creates a photocurrent and induces quasi-Fermi level splitting within the depletion region. The magnitude of the photocurrent depends on the thickness and absorption coefficient of the semiconductor. Figure 6.1 shows the absorption coefficients as functions of wavelength for various common semiconductors [2]. The absorption quickly rises once the photon energy is

greater than the bandgap. Also, direct band gap III-V semiconductors in general have at a least one order of magnitude higher absorption coefficient than indirect gap materials such as silicon. Therefore, a typical single-crystalline silicon solar cell needs to consume 10 times more volume (~ tens of μm thick) to achieve the same amount of photocurrent as its III-V counterparts (~μm thick).

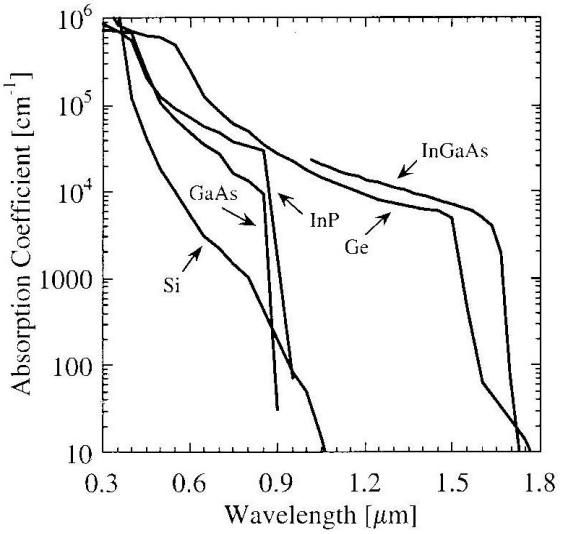


Fig. 6.1 *Absorption coefficient as a function of wavelength for several common Semiconductors [2]*

The quasi-Fermi level splitting in the depletion region is determined by the energy levels of the conduction electrons and holes. When a photon with energy larger than the bangap is absorbed, the created electrons or holes will first relax to the conduction or valance band edge, respectively, through heat dissipation before collected by the external load. Hence, the ceiling of quasi-Fermi level splitting is determined by the bandgap or Schottky barrier height of the device. For a solar cell based on a low bandgap semiconductor, its output voltage will be pinned by its low bandgap, although it can generate higher photocurrent due to its wider absorption range, and therefore the overall

power efficiency is reduced. The trade-off between absorption and quasi-Fermi level spitting determines the maximum available power efficiency of the solar cell by choosing the semiconductor with the optimal bandgap. The model for determining the limitation of solar cell efficiency is based on detailed balance proposed by Shockley et al [3]. In this model, only the radiative recombination is considered for electron/hole pairs within the solar cell, and the photocurrent is determined by assuming black body radiation from the sun (T=6000K). By considering the solid angle of solar illumination, estimated from the distance and diameter of the sun, the maximum power conversion efficiency of a homojunction solar cell is ~30%, shown in Fig 6.2 [3].

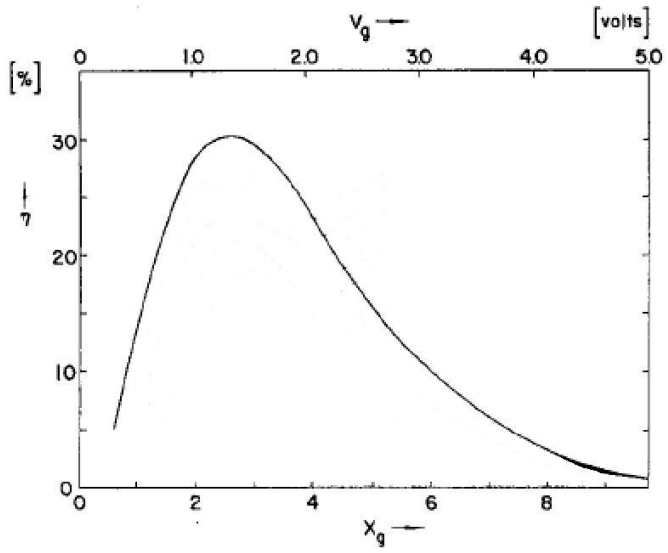


Fig. 6.2 *The optimum efficiency of solar cell determined by detailed balance limit. Here, v_g represent the bandgap, and x_g is the ratio between the bandgap and thermal energy at the surface of sun [3]*

Figure 6.3 is the ideal energy band profile of a p-n junction solar cell under illumination. The solar radiation is absorbed once it enters the semiconductor. The photocurrent is generated by collecting both the drifting carriers from the depletion

region and the minority carriers diffusing from outside of the depletion region but still within the carrier diffusion length. Since lightly-doped, single crystalline inorganic semiconductors in general have much longer diffusion length (typically > hundreds of μm) than the depletion width (typically < 10μm), most of the contribution to the photocurrent is from the diffusion of minority carriers.

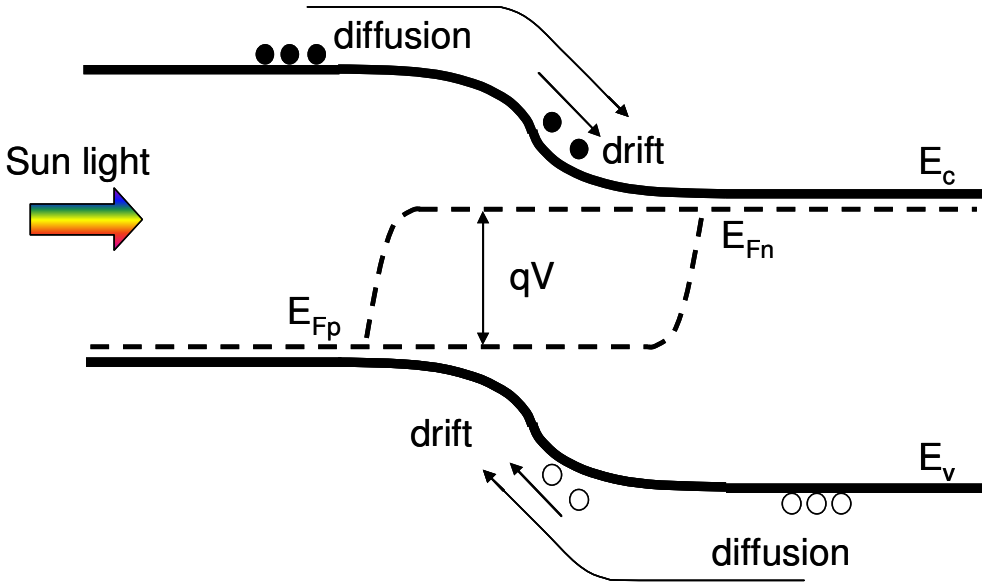


Fig. 6.3 *Energy band profile of the inorganic solar cell under illumination*

By including the resistive loss, the solar cell behavior can be described by the generalized Schottky equation based on the equivalent circuit model shown at Fig 6.4 [4]:

$$J = J_0 \exp\left[\frac{q(V - JR_s)}{nkT} - 1\right] + \frac{V - JR_s}{R_p} - J_{sc} \quad , \qquad (6.1)$$

where J_0 is the reverse saturation current density, n is the ideality factor, R_s is the specific series resistance, R_p is the shunt resistance, and J_{sc} is the photocurrent density. In general, J_0 is linearly proportional to $\exp(-E_g / kT)$, and is the saturation reverse dark current. The ideality factor n is between 1 and 2, and is determined by the whether the current is

dominated by diffusion (n=1) or non-radiative recombination (n=2). On the other hand, R_s is due to the finite conductivity of the semiconductor layer and metal stripes, and un-optimized ohmic contacts at the metal/semiconductor interface [5-6], while R_{sh} is related to the electric shunt path across the junction or the carrier recombination before being collected by electrodes.

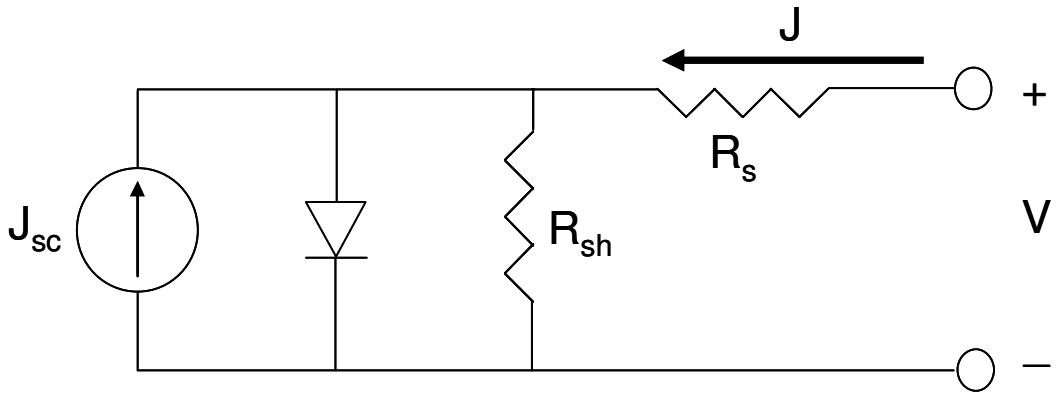
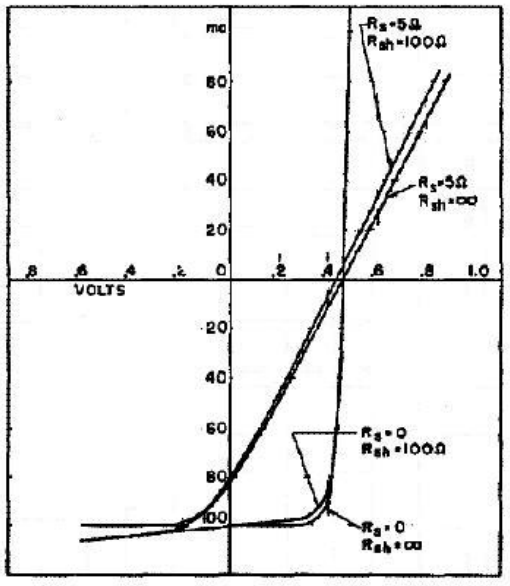


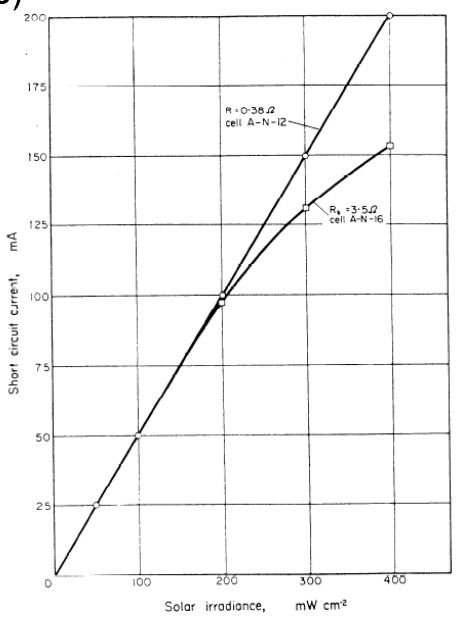
Fig. 6.4 *Equivalent circuit of an inorganic solar cell*

Based on Eq (6.1), the influence of R_s and R_{sh} can be seen from theoretical I-V characteristics of a silicon solar cell under illumination. The calculation shown in Fig 6.5(a) assumes R_s = 0 or 5 Ω and R_{sh} = ∞ or 100 Ω [7]. Surprisingly, both the fill factor and J_{sc} are dominated by R_s, while R_{sh} has negligible impact on the performance of the solar cell. This calculation is consistent with the measured roll-off of J_{sc} under high solar illumination, shown in Fig 6.5 (b) [8]. Figure 6.5 (c) summarizes the achievable electric power from a solar cell with various R_s [7]. With R_s increasing from zero to 10 Ω, the corresponding output electric power from solar cell drops to ~ 10% of its maximum output.

(a)



(b)



(c)

R_s	Relative maximum available power
0 ohms	1
1	0.77
2	0.57
3.5	0.37
5	0.27
10	0.14
20	0.07

Fig. 6.5 *(a) Theoretical I-V calculation with combination of various R_s and R_{sh} [7]*
(b) Measured I-V under various illumination intensity with two different R_s [8]
(c) Summary of the roll-off of efficiency with the increasing of R_s [7]

6.2 Characterization of solar cells

In general, the performance of a solar cell is evaluated by its power conversion efficiency and external quantum efficiency (EQE). The power conversion efficiency is characterized through the J-V characteristics under both dark and solar illumination conditions. Figure 6.6 is a schematic of the measurement setup for power efficiency measurements used in this work. The light source is a 150W Xe-arc lamp equipped with

air mass (AM) 1.5 global filter. The intensity of the light can be adjusted by choosing the appropriate neutral density filter. An NREL (National Renewable Energy laboratory)-calibrated silicon reference cell with diameter of 5mm is first used to determine the intensity of the light at the test position. Then, the light-intensity dependent J-V characteristics of the solar cell can be measured with an Agilent 4155B parameter analyzer.

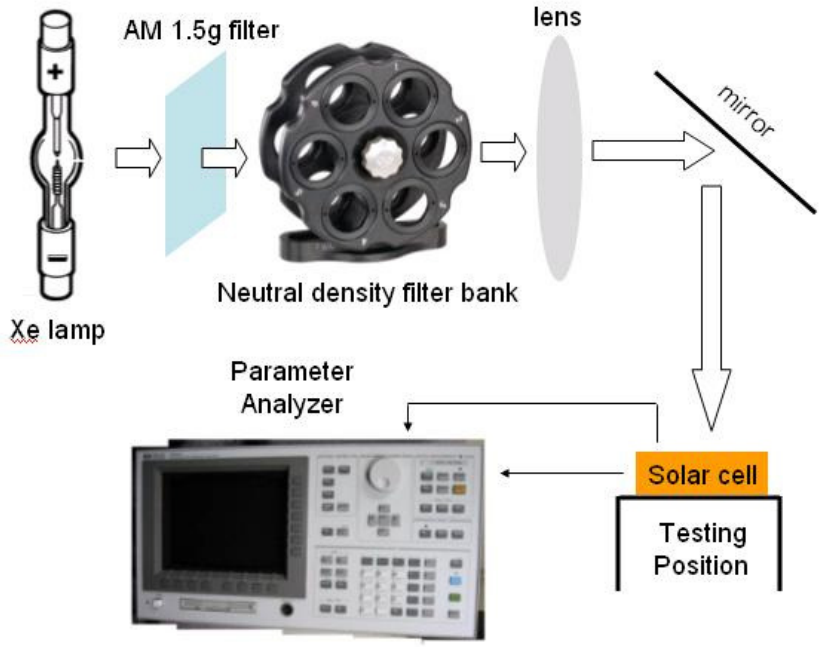


Fig. 6.6 *Schematics of power efficiency measurement setup*

From the measured light-intensity-dependent J-V characteristics, the open-circuit voltage (V_{oc}), fill factor (FF), and J_{sc} can be extracted to evaluate the performance of the test cell. For most of the single-crystalline InP thin-film solar cells tested in this work, J_{sc} is linearly proportional to the solar illumination from low intensity until at least few suns intensity. On the other hand, it is quite common to observe the roll-off the FF as the intensity of light increases due to high R_s. Hence, it is worthwhile to extract all of the

parameters described in the equivalent circuit in Fig 6.4 for complete analysis of the solar cell.

Analysis of solar cells requires a fit of the dark J-V curve to Eq (6.1) to obtain all of the circuit parameters. Alternatively, one can extract R_{sh} and R_s separately. Here, R_{sh} can be estimated by taking the derivative of the voltage v.s. current density under dark conditions, (-dV/dJ), and at reverse bias. R_s can be determined by comparing J-V curves under various illumination conditions [8]. From Eq (6.1), the shape of J-V curve will be distorted by R_s with $\Delta V = J.R_s$ drop as J_{sc} varies with different solar illumination intensities. As shown in Fig. 6.7 [5], R_s can be inferred from the skewed J-V curve under various illuminations by arbitrarily assigning a ΔJ for each of the J_{sc} [8]:

$$r_s = \frac{V_1 - V_2}{J_1 - J_2} \qquad (6.2)$$

where $J_1=J_{sc,1}-\Delta J$, and $J_2=J_{sc,2}-\Delta J$ with corresponding terminal voltage of V_1 and V_2.

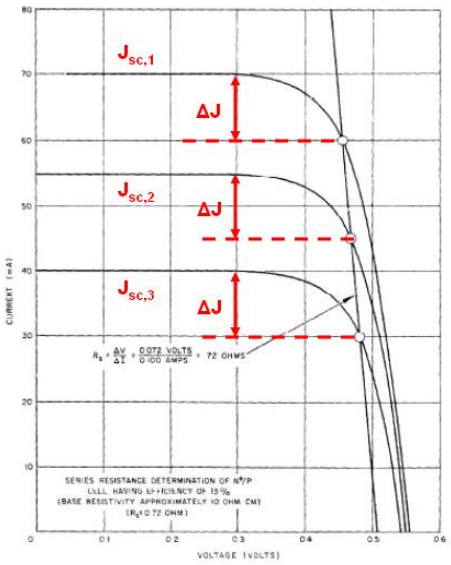


Fig. 6.7 *Series resistance determination of silicon n^+p cell [5]*

The EQE is defined as the ratio of the number of output carriers to the number of incoming photons as a function of wavelength. It is used to characterize the loss mechanisms of the photocurrent [9]. Sometimes the comparison between measured J_{sc} and the integration of EQE over the solar spectrum is used to verify the accuracy of the direct solar cell measurement. Figure 6.8 is the schematic of the EQE setup used in this work. White light coming from a tungsten halogen lamp is first input into a monochrometer. A band-pass filter is located at the output of monochrometer to cut off higher harmonics. The monochromatic light is then chopped at 200Hz, focused and aligned to the testing position. A lock-in amplifier is used to read the photocurrent from the test solar cell. The illumination intensity at the test position is first calibrated with a NIST traceable silicon reference photodetector. The EQE spectrum is then inferred by comparing the photocurrent spectrum of both the reference photodetector and the test solar cell.

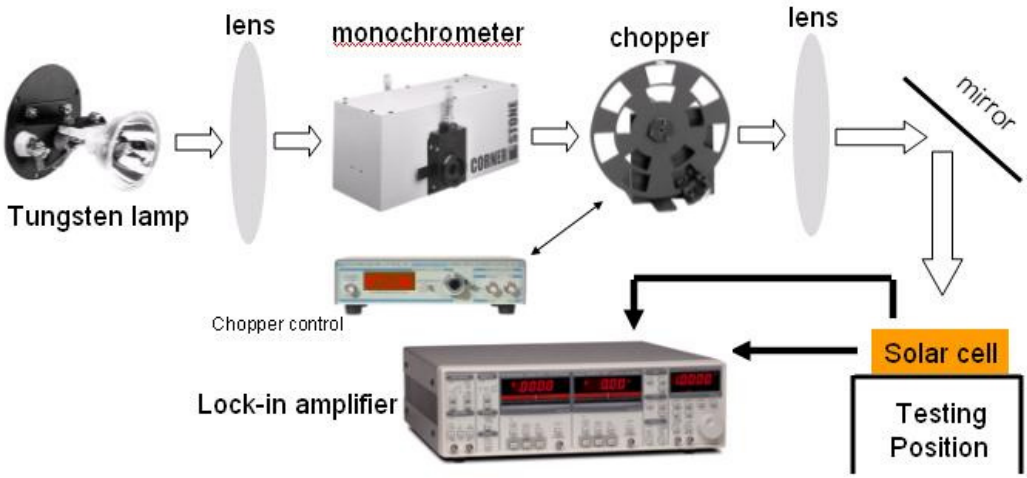


Fig. 6.8 *Schematics of EQE measurement setup*

The accuracy of J_{sc} measured from the power efficiency setup, shown in Fig. 6.6, can be determined by the EQE spectrum. The spectral mismatch factor, M, describes the photocurrent variation due to spectral variation between the AM 1.5G (the actual solar spectrum) and the filtered solar simulator [10-11], as follows:

$$M = \frac{\int_{\lambda_1}^{\lambda_2} E_{ref}(\lambda) S_R(\lambda) d\lambda}{\int_{\lambda_1}^{\lambda_2} E_{ref}(\lambda) S_T(\lambda) d\lambda} \frac{\int_{\lambda_1}^{\lambda_2} E_S(\lambda) S_T(\lambda) d\lambda}{\int_{\lambda_1}^{\lambda_2} E_S(\lambda) S_R(\lambda) d\lambda}, \qquad (6.3)$$

where $E_{ref}(\lambda)$ and $E_s(\lambda)$ are the spectrum of AM 1.5G and solar simulator, respectively, and $S_R(\lambda)$ and $S_T(\lambda)$ are the spectral responsivity of the silicon reference cell and test solar cell, respectively. For the power efficiency test setup used in this work, the spectral mismatch factor, M, typically lies between 0.92 and 1.02 over the wavelength 300nm< λ<900nm [11].

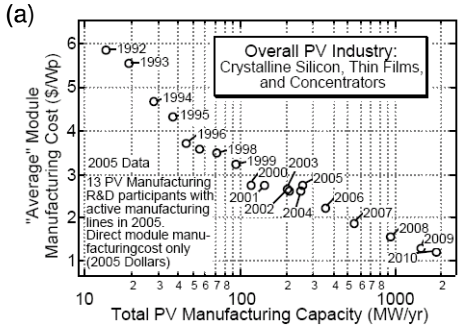
It is noted that the EQE depends on not only on the material absorption coefficient, α, but also the charge collection efficiency of the device. In this work, all of the test solar cells consist of lightly-doped, single-crystalline InP layers (typical diffusion length > few μm), and therefore the charge collection efficiency is typically independent of the bias and illumination intensity [9]. Nevertheless, if the solar cell material, such as a-Si, has a very short diffusion length (typically < 1μm), the photocurrent is primarily due to photon absorption in the depletion region, whose width highly depends on the applied voltage [9]. On the other hand, under high illumination intensity, due to the high densities of generated, the non-radiative recombination centers within the bandgap may be filled [12-13]. This results in enhancement of the minority carrier lifetime, therefore may over-estimate the charge collection efficiency. Solar cells with either a high defect density in the bandgap [9] or under ultrahigh illumination [12-13] have exhibited the illumination-

dependent EQE. Since the typical light intensity for an EQE testing setup is several orders of magnitude lower than the concentrated solar illumination, it may be necessary to apply a biased d.c.white light superimposed on the chopped monochromatic light for characterizing those cells [13].

6.3 Cost analysis of III-V thin-film solar cells

There has been significant efficiency improvements and cost reduction for various photovoltaic (PV) modules over the last few decades. Figure 6.9 (a) shows the progress of the evolution of overall manufacturing cost of PV modules in the U.S. between 1992 and 2005 [14]. Within this period, the average production cost decreased at the rate of 5.7% per year [14]. In fact, the actual module cost may vary from technology to technology. Figure 6.9 (b) is an estimation of the production cost of selected mainstream technologies in the current PV industry [15]. Generally, the thin-film PV module production cost lies between \$1.0-\$2.5/W_p. On the other hand, Fig 6.9 (b) does not include III-V semiconductor-based PV modules, as the developing of III-V thin-film solar cell is still in its infancy. To estimate the production cost of future III-V thin-film PV modules, it is necessary to consider all aspects of the manufacturing, which includes but is not limited to raw material consumption, utilities usage, equipment maintenance, fabrication processes, and labor [16]. Since the development of III-V thin-film PV is still in its infancy, the actual production cost cannot be accurately forecasted. Therefore, in this chapter, we will only consider the intrinsic factors, namely, the usage of raw materials, to estimate the production cost.

(a)



(b)

Module Price, Manufacturing Cost, and Efficiency Estimates by Technology, 2008

Technology	Price (2008 $/Wp)	Manufacturing Cost (2008 $/Wp)	Conversion Efficiency
High-efficiency monocrystalline silicon	$3.83	$2.24	17.5%
Multicrystalline silicon	$3.43	$2.12–$3.11[40]	13.5%
Amorphous silicon (a-Si) thin film	$3.00	$1.80	6.5%
Copper indium diselenide/copper indium gallium diselenide (CIS/CIGS) thin film	$2.81	$1.26	10.2%
Cadmium telluride (CdTe) thin film	$2.51	$1.25	10.0%
Mehta and Bradford 2009			

Fig. 6.9 *(a) of the evolution of overall manufacturing cost of PV modules at U.S. [13] (b) The manufacturing cost of various PV module at the year of 2008 [14]*

The scenario we are going to consider is to fabricate solar cell devices with GaAs thin-film (grown by MBE or MOCVD) on kapton sheets and GaAs substrates, and polycrystalline silicon thin-film on the glass sheets. To simplify the calculation, we assume that the epitaxial structure of both GaAs [17] and polycrystalline silicon thin-film solar cell [18] only contains 2μm of undoped base layer while that of bulk, conventional GaAs solar cell is 4μm. Table 6.1 illustrates the wholesale price of various raw materials for the making solar cells. The material usage efficiency of each process gas or metal ingot depends on the characteristics of the tool used for the epilayer growth. Standard PECVD, used for depositing thin-film silicon, has a gas utilization efficiency of about 8% [19], while III-V MOCVD typically exhibits deposition efficiency of around 40% [20]. On the other hand, the material usage efficiency of MBE is estimated to be 12% for metal ingot and 9% for group V solid source by the estimated annual production data from a

typical Veeco GEN 2000 production MBE. It is very likely that the exact MBE material efficiency is much higher than the numbers used here, as this estimation cannot preclude the influence coming from the non-optimized human operation procedure and production management. Compared to PECVD and MOCVD, MBE also requires extra supply of liquid nitrogen (LN_2) to cool down its chamber to achieve high vacuum. Based on the specifications for the Veeco GEN 2000 system, the typical consumption rate of LN_2 is about 150 per hour for the growth on fourteen pieces of 4-inch wafers at the same time. The usage of gallium ingots, arsine gas, and LN_2 in the MBE system will contribute the production cost of the solar cells.

Raw material	Price	Note
Gallium Ingot (6N)	$2.65/gram	Ingot volume :10 Kg
Trimethylgallium (TMGa) (gallium : 60.7 wt%)	$12/gram ($20/one gram of gallium)	Fill weight : 1000 gram
Arsine	$2.1/gram	Fill weight : 0.5 pounds
Arsenic	$0.9/gram	Volume: 10 Kg
Silane (5N)	$0.33/gram	Fill weight : 5 Kg
GaAs wafer (4 inch diameter)	$ 225	Buy 100 pieces a time
Glass plate ($0.57\ m^2$)	$35	Price inferred from cost Structure of LCD panel
Kapton sheet (125μm thick)	$75/m^2	Year of 2010
Liquid nitrogen (LN_2)	$0.09/liter	Price inferred from monthly cleanroom usage at U of Michigan.

Table. 6.1 *The summary of price of raw materials for solar cells.*

Table 6.2 illustrates the details of the cost estimation. Each solar cell is assumed to be operated at the corresponding highest reported efficiency [17-18], and the usage of the process gas and ingots is calculated based on the volume and density of the epitaxial layer. Here, the substrate size of each III-V cell is based on the maximum wafer loading capacity of current commercially available MBE tool. The growth rate of GaAs is assumed to be 1μm/hr. For MOCVD, the V/III ratio is assumed to be 20. Apparently, the production cost of a conventional GaAs cell is determined by the cost of GaAs wafer and therefore is several orders of magnitude higher than its thin-film type cell. The cost of each individual thin-film type cell is determined by the species of production gas and ingots. Therefore, due to the expensive high-purity TMGa gas, the growth cost of the MBE-grown GaAs thin-film is more competitive than the MOCVD-grown devices but still more expensive than silicon thin-film cells made using silane. On the other hand, the typical production cost of the conventional, bulk, single-crystalline silicon solar cell is estimated to be ~ $5.0/Wp by considering the typical price of an 8-inch silicon wafer (~ $40), and the optimal efficiency of the silicon cell (~ 25%). Hence, based on the cost analysis from Table 6.2, GaAs thin-film solar cell will be cheaper than conventional single-crystalline silicon bulk solar cells after reusing a single GaAs wafer more than 36 times. This will at least allow the PV market to enjoy the high efficiency III-V tandem solar cells by paying a similar cost as conventional silicon solar cells, while there is no fundamental physical limit to keep reusing the same GaAs seed wafer. Nevertheless, the cost of III-V thin-films can be further reduced by adopting high-efficiency tandem structures, and developing large-diameter III-V wafers and its corresponding production tool.

PV module	Si on glass by PECVD	GaAs on plastic by MBE	GaAs on plastic by MOCVD	GaAs on GaAs by MBE
Best efficiency	10.7% [5]	26.1% [4]		
Material usage	Si : 2.66 gram	GaAs: 1.17 gram		2.34 gram
Substrate	Glass 0.57m^2	Kapton, 0.11m^2	Kapton, 0.11m^2	GaAs, 0.11m^2
Tool efficiency	Silane : 8%	Ga Ingot :12% Arsenic : 9%	TMGa :40% Arsine : 2%	Ga Ingot :12% Arsenic : 9%
LN_2 consumption	None	300 liter	None	600 liter
Cost of material	$ 11	$ 19	$ 92	$ 38
Cost of substrate	$ 35	$ 8	$ 8	$ 3150
Cost of LN_2	none	$ 27	none	$54
Total Cost ($/m^2)	$ 81	$ 491	$ 909	$ 29564
Total Cost ($/Watt)	$0.76	$ 1.86	$ 3.44	$ 112

Table 6.2 *The estimated production cost of various solar cells*

(Note: The typical Veeco GEN II can load fourteen, 4-inch wafers at a time. Hence, in this table, the area of GaAs cell is estimated to be 0.11m^2. The Si cell is assumed to be 0.57 m^2, which is approximately equal to the size of 42-inch LCD panel.)

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Chapter 7

GaAs MBE growth on insulating substrates

7.1 Introduction

In this chapter, we will first review the past work on poly-crystalline III-V thin-films. Then, we will address this challenge by growing polycrystalline GaAs on quartz substrates via droplet epitaxy and selective epitaxial growth by molecular beam epitaxy (MBE). Droplet epitaxy determines the density of initial GaAs nuclei, while the subsequent GaAs selective epitaxial growth permits grain growth on the existing nuclei. The GaAs thin films are characterized by atomic force microscopy, x-ray diffraction and scanning electron microscopy. By adjusting the gallium droplet density and substrate temperature, we have achieved poly-crystalline GaAs with cluster sizes > 700nm and grain size > 100nm oriented along the (111) crystal plane, as compared to 50nm diameter cluster and (111) crystal plane size of 40nm achieved by conventional MBE growth.

7.2 Review of poly-crystalline III-V thin-film growth on glass

Since the successful demonstration of the growth of amorphous silicon (a-Si) thin-films in the 1970s [1-2], numerous commercial a-Si-based device applications, such as active matrix liquid crystal displays (AMLCD) and solar cells [3] have emerged in the market. In contrast to the success of a-Si, the research progress of amorphous III-V is still in its infancy, because the primary bottleneck is the difficulty in achieving intentional doping in amorphous III-V [4]. The compensation ratio Q, defined as the ratio of the concentration of free carriers to the donor-defect pairs, is given by [4]:

$$Q = D/n = Q_0 \exp(\frac{\Delta - H}{k_B T}) \qquad (7.1)$$

where D is the density of defects, n is the free carrier concentration, Δ is the compensation energy, and H is the enthalpy of the amorphous semiconductor. In general, H is a function of by the cohesive energy per atom, and lies at the range of 0.6eV – 1.1eV for amorphous silicon and most III-V materials [4]. On the other hand, dangling bonds residing in amorphous semiconductors result in defect levels in bandgap. When incorporating donors into the amorphous thin-film, instead of releasing electrons to the conduction band-edge, donors have a tendency to form donor$^+$-defect$^-$ pairs to gain compensation energy, Δ [4]. As indicated in Fig 7.1 [4], the energy of a silicon dangling bond in a-Si is about 0.8eV below the conduction band edge [5], while the dangling bond of arsenic in a-GaAs creates defect levels close to the valance band-edge [6]. Hence, donors gain larger compensation energy in amorphous III-V materials than in a-Si. Therefore, the compensation ratio, defined as the ratio between the concentration of free carriers and donor-defect pairs, is predicted to be larger than 10^8 while that of a-Si is only 10 [4]. The same principle can be applied to the case of acceptor doping. This explains why it is not feasible to make electronic devices with amorphous III-V semiconductors while numerous a-Si-based applications have been commercialized.

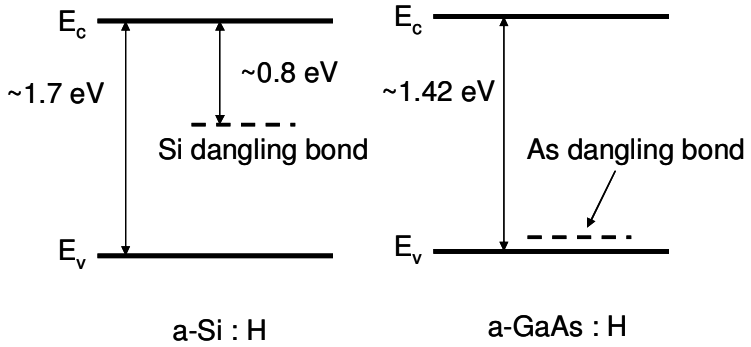

Figure 7.1 *The band profile of a-Si and a-GaAs with defects level contributed by dangling bonds[4]*

On the other hand, poly-crystalline thin-films preserve crystallinity within a grain, confining dangling bonds to the grain boundaries. Figure 7.2 is the band diagram of an n-type poly-crystalline semiconductor near a grain boundary [7]. Similar to the case of an amorphous semiconductor, the electrons released from the donors close to the grain boundary are captured by defects states. This induces a space charge region and causes the polycrystalline grain to be surrounded by a barrier of height, E_b [7]. This barrier increases the resistance of the n-type thin-film, and may block the conductivity if the space charge region is larger than the size of the polycrystalline grain. Therefore, it is necessary to enlarge the grain size to realize intentional doping.

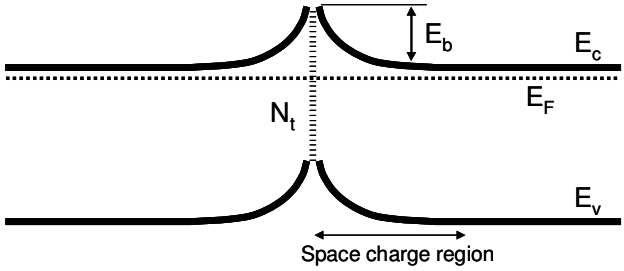

Figure 7.2 *The band profile of a n-type poly-crystalline semiconductor near the grain boundary [7]*

The common technique of grain growth to convert the amorphous thin-film to a polycrystalline network is through either solid-phase crystallization [8-9] or pulse-laser-annealing [10-11]. Solid phase crystallization employs continuous thermal annealing at temperatures of around 600^0C for several hours. Its working principle is based on the assumption that the activation energy of grain growth is lower than that of nucleation [12]. For a-Si, the activation energy of nucleation and growth, determined by bulk-induced and surface-induced crystallization, is about 9 eV and 2.4 eV, respectively [13]. Therefore, a-Si is a suitable material for solid-phase crystallization [8-9]. However, solid-phase

crystallization has nearly no effect on GaAs grown on a quartz substrate [14]. Although Yokoyama, et al. reports an ultra-low activation energy of GaAs crystal growth of 0.6 eV when the annealing temperature is above 400^0C [15], there is no guarantee that this experiment completely decoupled the contribution from grain growth and nucleation, as suggested in [13]. Based on the result from [14], it is reasonable to speculate that the activation energy of GaAs nucleation is close to or even lower than that of crystal growth. Pulse-laser-annealing utilizes a short-wavelength laser to nearly completely melt the amorphous thin-film while leaving behind some solid seeds located at the interface of the thin-film/glass substrate. During cooling, the crystallization starting from those buried solid seeds allows the formation of larger polycrystalline grains. Despite the successful demonstration of pulse-laser-annealing of a-Si, less success has been achieved for III-V materials. Pirzada et al [15] demonstrate that the grain size of poly-GaAs after KrF excimer laser annealing is still below 0.5 μm. One possible cause is the rapid formation of new nucleation sites during the cooling following of the pulse laser.

Currently, the most successful work of growing polycrystalline III-V thin-film is through direct epitaxy. A GaAs cluster size of 0.5 μm achieved with chemical beam epitaxy (CBE) [16] and a grain size of 1-10 μm with MOCVD [17-18]. In this chapter, we will investigate the possibility of having large polycrystalline grains of GaAs thin-film grown on insulating substrates via direct growth with MBE.

7.3 Growth of polycrystalline-GaAs on sapphire substrates

Sapphire (0001) is firstly selected as the substrate material for the growth of polycrystalline GaAs. The GaAs thin-films are grown on sapphire (0001) substrates via

gas-source molecular beam epitaxy. Before the growth, the sapphire substrate is dipped in hot trichloroethene for 10 mins, acetone for 5 mins, and hot iso-propanol for 5 mins, and then mounted on the indium-free holder with a 3-inch silicon as its diffuser plate. During growth, the sapphire substrate is heated by thermal contact from the silicon plate which absorbs the infrared from the substrate heater. The substrate temperature is read by the thermocouple located at the back of the indium-free holder.

Figure 7.3 (a)-(b) is the AFM image, SEM image, and the θ-2θ XRD scan of 600 ML thick GaAs thin-film directly grown on sapphire via MBE with the GaAs growth rate of 0.3 ML/sec (V/III ratio > 20) and substrate temperature of 50^0C and 400^0C, respectively. For the sample grown at 50^0C, AFM reveals morphology indicative of nanocrystalline growth. It is consistent with the XRD scan which shows no obvious epilayer diffraction peak and weak X-ray counts due to the x-ray scattering from the substrate surface. When the growth temperature is increased to 400^0C, the surface mobility of gallium adatoms increases [19] and therefore the grain size increases to 200nm. The θ-2θ XRD scan reveals diffraction from (111) GaAs plane with other minor diffraction from other crystalline facets such as (220) or (311). Since diffraction from (111) GaAs plane has the strongest intensity, all of the XRD-related characterization in the chapter will be only applied to (111) peak.

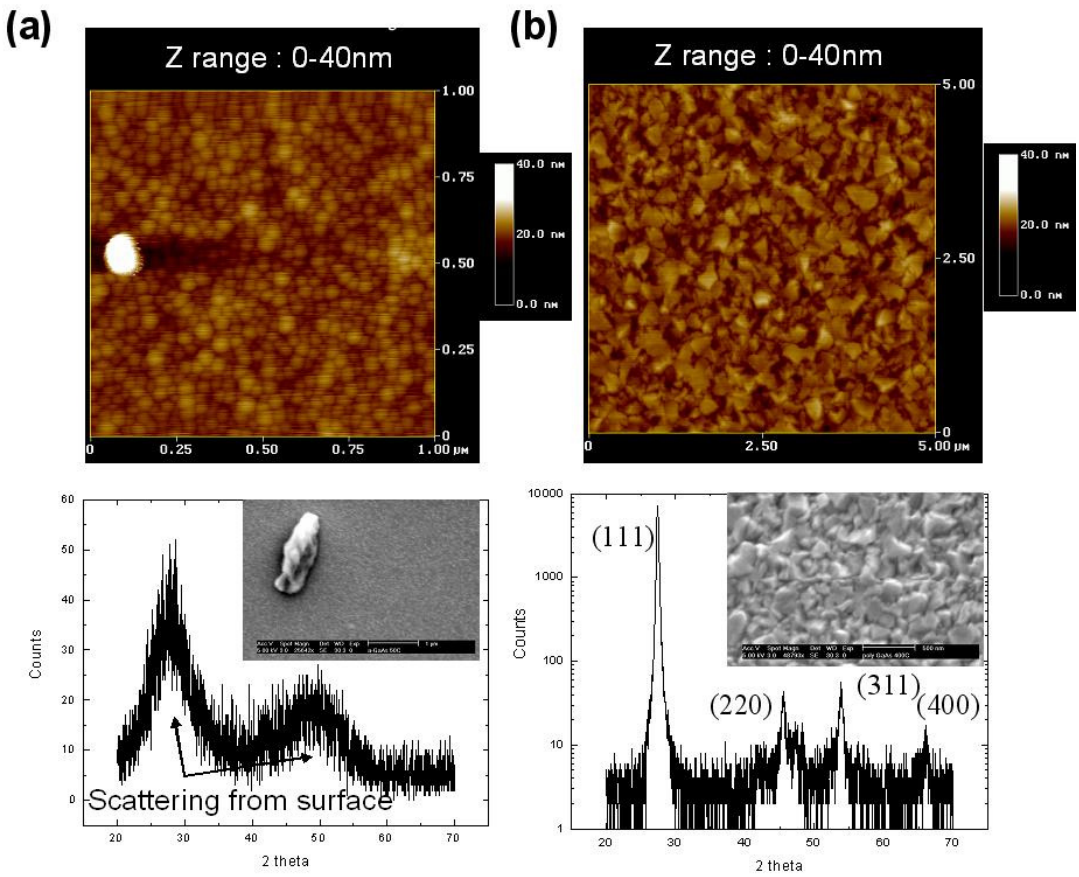

Figure 7.3 *The AFM image (Z range is between 0 and 40 nm), SEM image, and θ-2θ XRD pattern of polycrystalline GaAs thin-film grown on sapphire (0001) at the growth temperature of (a) 50^0C (b) 400^0C on quartz substrate.*

Nevertheless, if further increases the growth temperature, instead of increasing the grain size, the growth mode of GaAs film transforms to island growth. It is likely that much higher substrate temperature allows adatoms to completely perform the epitaxial growth determined by the crystallinity of sapphire substrate [20]. Figure 7.4 is the SEM image pyramid shape GaAs islands grown at the substrate temperature of 550^0C. The corresponding coarse XRD scan exhibits only diffraction from (111) and (222) planes, which suggests the strain between GaAs and sapphire substrate enables the 3D growth mode.

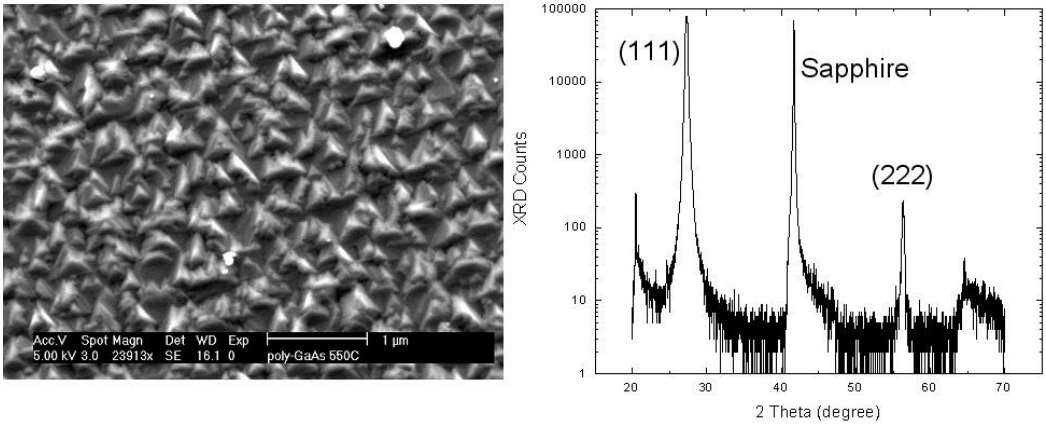

Figure 7.4 *The SEM image, and θ-2θ XRD pattern (taken at XMAL at U of Michigan) of polycrystalline GaAs thin-film with 0.35µm thick grown on sapphire (0001) at the growth temperature of 550^{0}C*

Although thin-films with 3-D islands morphology are not favorable for most optoelectronic device applications, it is worthwhile to investigate the possibility to utilize these islands as the initial seed layer for the polycrystalline grain growth afterwards. Similar concept has been demonstrated by Allen et al. [21], at which the nanolithography patterned gallium balls serve as nucleation sites of polycrystalline GaAs film on silicon substrate. Here, the growth sequence firstly starts from depositing 100ML of GaAs at the substrate temperature of 600^{0}C to form 3-D GaAs islands. The substrate is then cooled down to 400^{0}C and is deposited with 2400 ML of GaAs at the growth rate of 0.3ML/sec. Finally, these samples are covered with 200nm of SiO_x and annealed under vacuum at 600^{0}C/ 700^{0}C for 20 hours. The AFM morphology and FHWM of XRD scan will be used to reveal the result of grain growth before and after the thermal annealing. Figure 7.5 illustrates the AFM surface morphology and the corresponding XRD scans of the seeded GaAs layers following various grain growths and annealing steps, while similar data for the unseeded GaAs layers is shown in Fig 7.6. For the samples with seed layers, only (111) diffraction is exhibited after the annealing, while that without seed layer still shows

various crystal planes. Both set of samples show reduced FWHM of XRD diffraction from (111) plane after annealing. This implies that the GaAs grains either coalesce with the islands from the seed layer or with each other (when there is no seed layer underneath) during the high temperature annealing. Further increasing the annealing temperature has proved to cause significant arsenic loss from GaAs thin-film and therefore the surface of samples becomes totally milky.

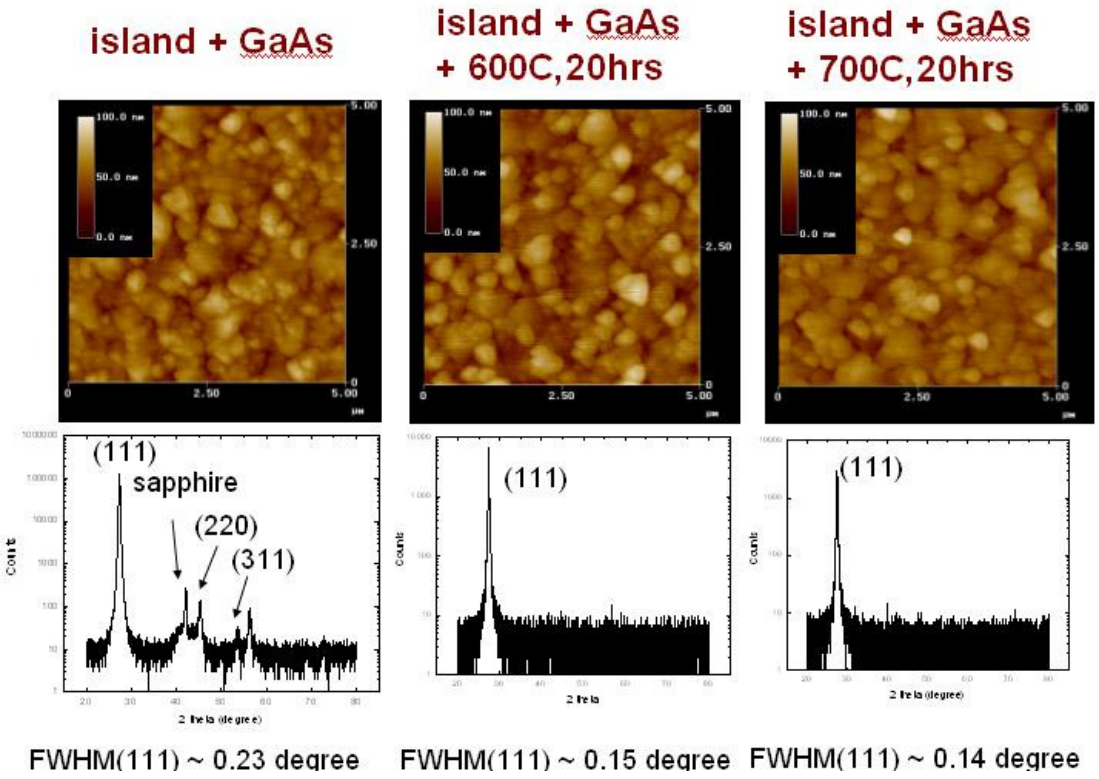

Figure 7.5 *The AFM image, and coarse XRD pattern of annealed polycrystalline GaAs layer grown on the GaAs seed layer at the 400^0C*

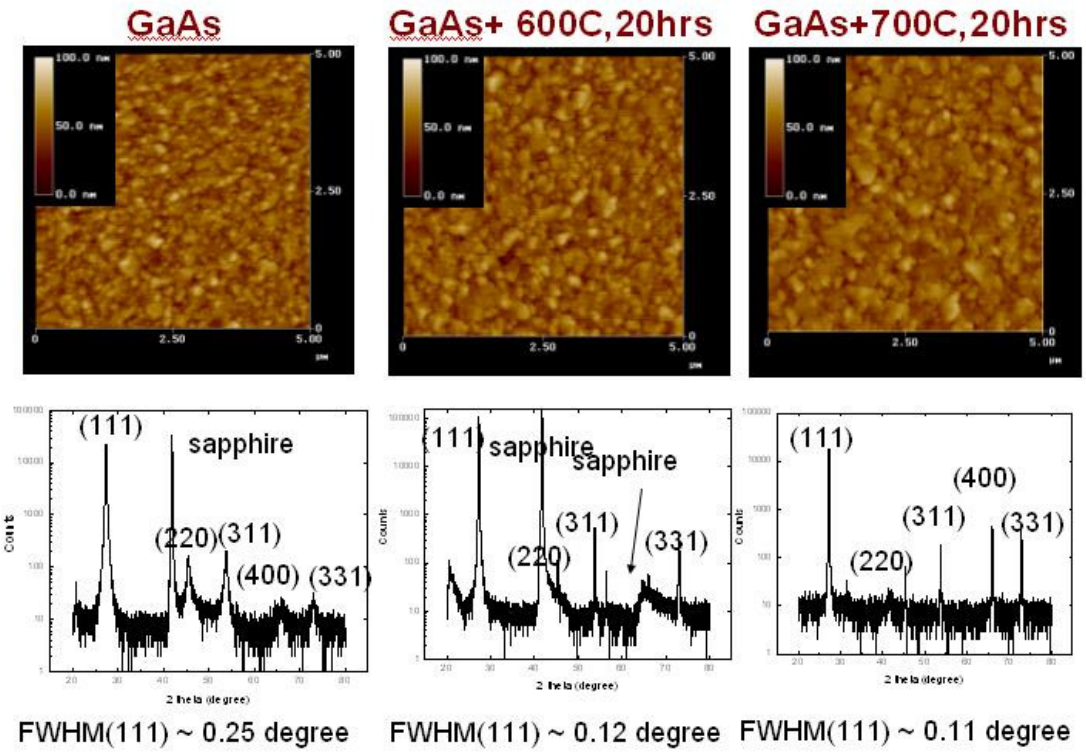

Figure 7.6 *The AFM image, and coarse XRD pattern of annealed polycrystalline GaAs layer at 400^0C*

7.4 Growth of polycrystalline-GaAs on quartz

In the previous section, we discussed the growth polycrystalline GaAs on sapphire substrate. Typically, the cost of sapphire plate and GaAs wafer are very similar. Therefore, it is worthwhile to consider the growth of polycrystalline GaAs on cheap, amorphous quartz plates.

The procedure of the surface pretreatment of quartz substrate is the same as that described at the previous sector. During the growth, the substrate temperature is read by the thermocouple at the back side of the indium-free block. To ensure the reproducibility of the growth, the corresponding temperature readout from pyrometer, previously

calibrated by using GaAs substrate during the desorption of its native oxide, is also recorded.

The procedure of MBE grain growth consists of two parts – one is to initiate the GaAs seed layer, and the other is to perform selective epitaxial growth on the existing GaAs islands to enlarge the size of GaAs polycrystalline grains. Figure 7.7 represents the procedure of grain growth. First, gallium clusters are grown on the surface of quartz substrate held at a moderate temperature (~ 500^0C) by supplying few monolayers of gallium adatoms. Those gallium clusters are later converted into GaAs islands by interacting with the incident arsenic dimers provided by the injected arsine at a flow rate of 2 sccm through the gas cracker. Then, the substrate temperature is raised to 850^0C for the subsequent selective epitaxy. For a given arsenic flux, higher substrate temperature can increase both the surface diffusion length and the desorption rate of gallium adatoms [19,22], and therefore is capable of realizing selective GaAs epitaxy growth because the incoming gallium adatoms will either quickly re-evaporate from the quartz substrate before interacting with arsenic dimers, or diffuse to neighboring GaAs seeds. This prevents the formation of new GaAs nuclei on the quartz surface, enlarges the size of the existing GaAs islands, and therefore, the final grain size should be highly dependent on the spacing of the initial GaAs islands.

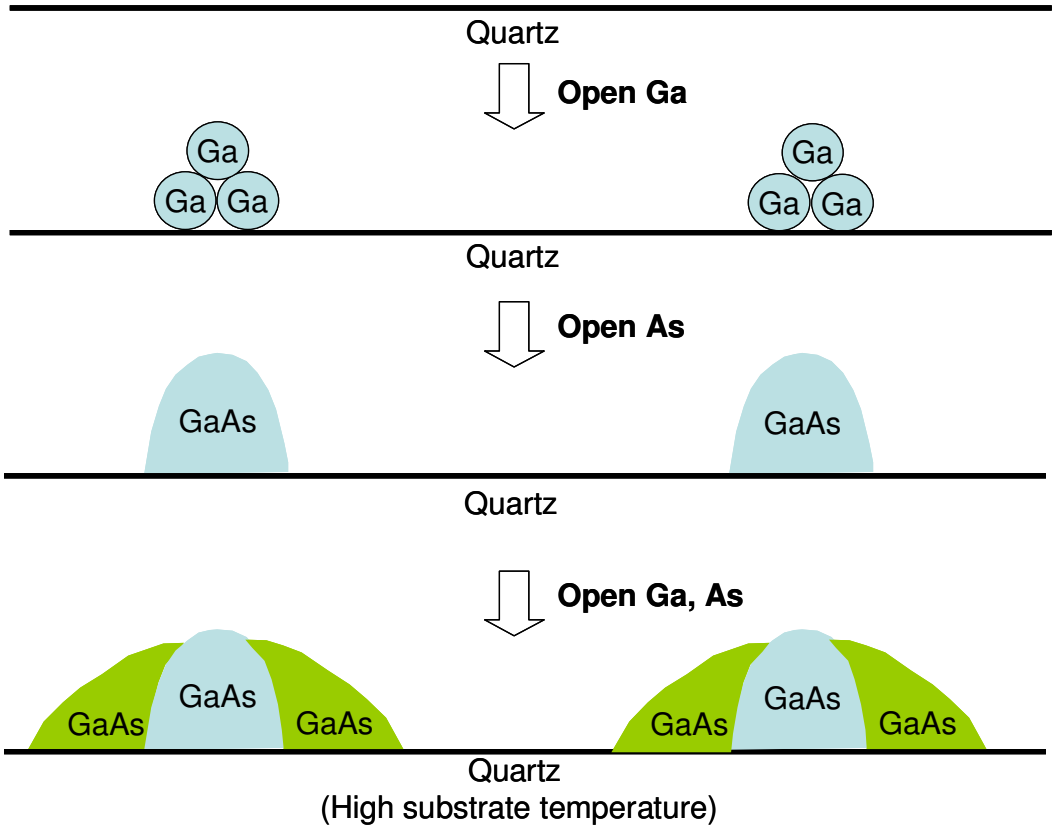

Figure 7.7 *The idea of poly-crystalline GaAs grain growth with MBE. The density of the nuclei is determined by the initial density of gallium droplets. The selective area epitaxy will enlarge the existing GaAs island while prohibiting the formation of the new GaAs nuclei.*

Figure 7.8 (a) is the AFM image of a 600 ML thick GaAs thin-film directly grown on 600^0C quartz via MBE. Apparently, the grain size is less than 50nm. The coarse XRD scan, shown in Fig 7.8 (b), exhibits peaks from multiple crystal planes, which indicate poly-crystallinity. Figure 7.8 (c) is the high resolution XRD scan of the (111) plane with a full-wide-half-maximum of 0.224^0. After considering the resolution of the XRD setup determined by the FWHM of the XRD scan of a single-crystallne GaAs (111) wafer, the crystal size, estimated from the Scherrer equation [23], is about 50nm. This is consistent with AFM image.

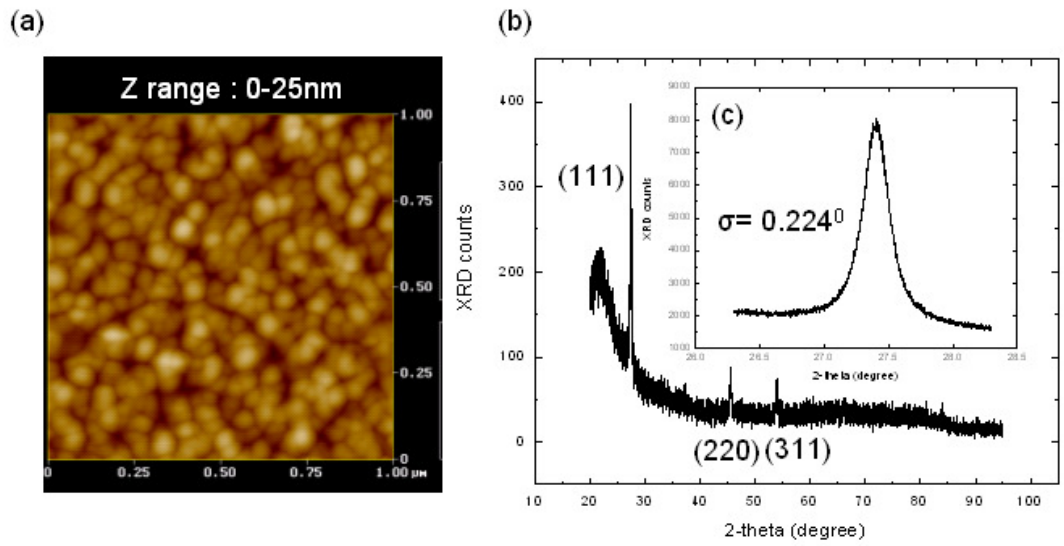

Figure 7.8 *(a) The AFM phase image, (b) the coarse XRD pattern, and (c) the fine XRD scan at (111) plane of the as-grown GaAs thin-film (600ML thick) on quartz substrate.*

Figure 7.9 (a) is the AFM image of the grain growth after seeding with 6 monolayers (ML) of GaAs at a rate of 0.2 ML/sec, followed by the selective GaAs epitaxial growth of 1000ML at 850^0C. Based upon AFM image, the size of the resulting GaAs clusters is approximately 700nm, consistent with results from the SEM image, shown in Fig 7.9 (b). The XRD pattern along the (111) plane, exhibited in Fig 7.9 (d), implies that the grain size is about 93nm. Figure 7.9 (d) illustrates the comparison of the growth with and without initial GaAs islands. This shows that high substrate temperature supports selective epitaxy, and therefore the growth can only occur on the pre-deposited GaAs islands.

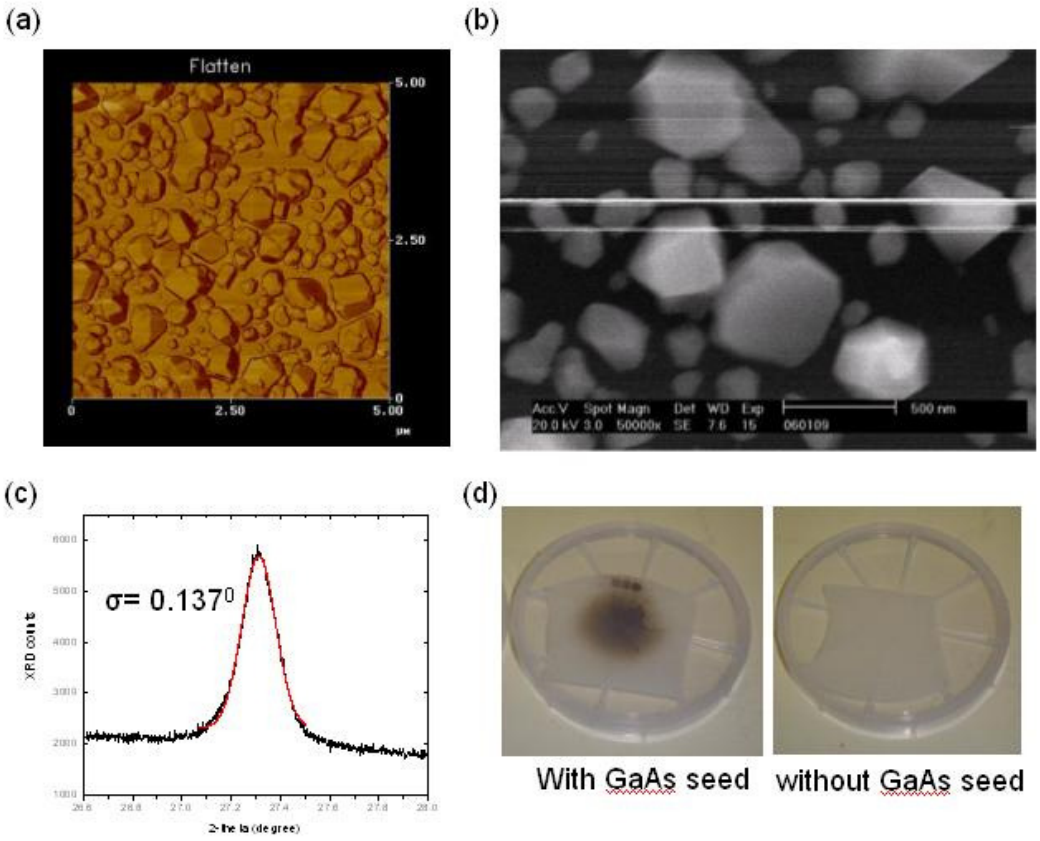

Figure 7.9 *(a) The AFM image, (b) the SEM image (c) the fine XRD scan at* (111) plane *of the GaAs growth (1000ML thick) at 850C with the initial GaAs seed layer(6ML thick)*(d) The photo of the GaAs selective epitaxy with and without the initial GaAs see layer.

To verify the influence of the GaAs islands, we reduce the thickness of the initial GaAs seed from 6ML to 4 ML and then grow 2000ML of GaAs with the same recipe as discussed earlier. It is originally expected that the final grain size can be further enlarged based on the concept at Fig. 7.7. However, as shown in Fig 7.10 (a)-(b), the size of the GaAs cluster and grain only exhibits slight improvements compared to Fig 7.9 (a)-(c). Figure 7.11 is a plain view TEM image of the GaAs clusters shown in Fig 7.9 (a)-(c). Apparently, there are twin structures located within each GaAs cluster, resulting in actual grain size smaller the cluster size. We speculate that the initial GaAs seeds are

aggregation of clusters which may limit the final grain size following selective epitaxial growth.

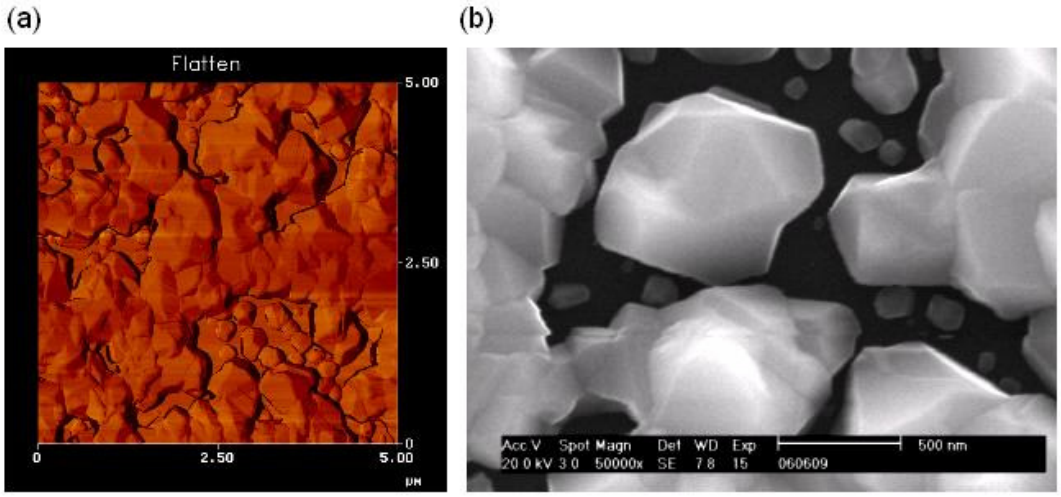

Figure 7.10 *(a) The AFM phase image, (b) the SEM imaging of the GaAs growth (2000ML thick) at 850C with the initial GaAs seed layer(4ML thick).*

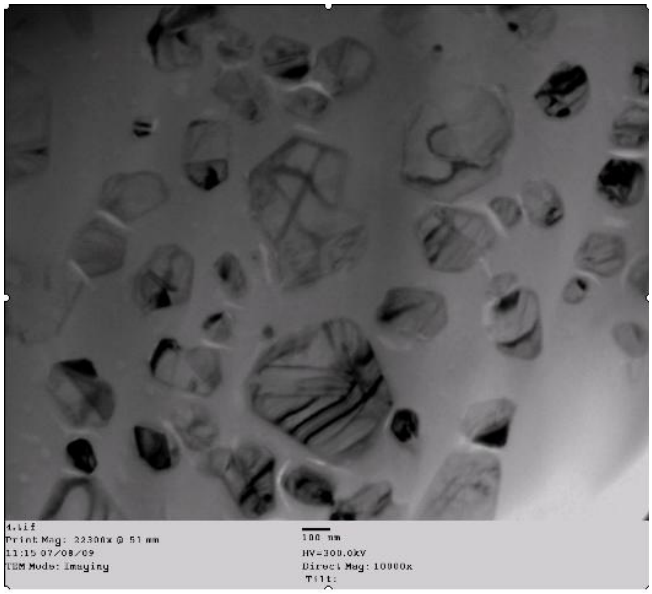

Figure 7.11 *The plain TEM image of the GaAs growth (1000ML thick) at 850C with the initial GaAs seed layer(6ML thick). The sample preparation includes thinning the quartz substrate to 25 µm followed by the ion milling.*

7.5 Conclusion

In this chapter, we demonstrate the grain growth of polycrystalline GaAs on an insulating sapphire and quartz substrate. The growth on sapphire becomes polycrystalline when the substrate temperature is above 400^0C. The resulting 3-D GaAs islands determine the final clusters size, which is less than 500nm. On the other hand, by combining the technique of droplet epitaxy and selective epitaxy, the resulting size of GaAs clusters on amorphous quartz plates is around 700nm, while XRD indicates that the grain size is approximately 100nm. TEM images show the possible existence of grain boundaries within each GaAs clusters. The polycrystalline GaAs growth with n-type intentional doping has been performed on both sapphire and quartz. Nevertheless, both samples exhibit no current readout during Hall measurement which indicates the nature high resistivity. This indicates that the GaAs grain size still needs to be further enlarged to overcome the free carrier compensation before it is useful for solar cell applications.

Future work should be focused on optimizing the GaAs nuclei by decreasing the GaAs deposition rate, increasing the annealing temperature, or adopting other alien seed layers for GaAs growth on quartz substrates. The resulting grain size has to be larger than 5-10 μm to achieve a solar cell of efficiency of 2%-5% [17-18] or mm to have the compatible efficiency as III-V single-crystalline solar cells [24]. Nevertheless, considering the typical III-V thin-film growth rate of 1μm per hour, it is expected that millimeter grains will require at least several hundred hours of growth even if the scheme of single crystalline III-V nuclei and completely selective, lateral growth is achievable. Therefore, to fully realize high efficiency III-V thin-film solar cells, direct bonding will be a favorable and economical alternative to direct growth.

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Chapter 8

InP thin-film solar cell on flexible plastic substrates

8.1 Introduction

While the progress of III-V hetero-epitaxy either from the solid phase or direct growth is still in its infancy, an alternative way to realize III-V thin-film solar cells is through direct bonding of a pre-grown single-crystalline epitaxial layer film onto a foreign substrate. To achieve low production cost, it is eventually required to reuse the original III-V parent or seed substrate, followed by fabricating the thin-film solar cells onto the foreign (e.g. plastic) substrate with direct bonding. However, before demonstrating the method of reusing the original III-V substrate, this chapter will focus on realizing and characterizing the performance of a III-V thin-film solar cell. Here, InP Schottky-type junctions are selected as the solar cell structure because of its ease of fabrication. The original InP substrate is then removed via etching. Although the step of sacrificing the entire InP substrate is far from the scheme of low production cost, the resulting ITO/InP thin-film solar cell is capable of high power conversion efficiency (~10%), high specific power because of the low weight of the plastic substrate (~2.0 kW/kg), and high flexibility which can tolerate both tensile and compressive stress by bending over a <1 cm radius without damage.

8.2 Band alignment at ITO/InP Schottky junction

The conventional Schottky-type InP bulk solar cell, demonstrated by Coutts, et.al. [1], has been shown to have a efficiency of ~ 19% under 1 sun illumination. This is somewhat inferior to the p-i-n InP homojunction solar cell with an efficiency of 22% [2]. However, Schottky-type InP bulk solar cells are promising due to its their ease of fabrication: namely, they only require metallization for the back contact and indium-tin-oxide (ITO) sputtering on the front side of the bare, lightly p-doped InP wafer.

The working principle of such a solar cell relies on the large Schottky barrier height at the interface between the ITO contact and the p-doped InP substrate. Based on the principle of ideal band alignment, called the Schottky limit, the Schottky barrier height, ϕ_B, is determined by the alignment between the work function of the metal contact, ϕ_m, and the Fermi level, ϕ_F,of the bulk semiconductor. In practice, ϕ_m has the tendency to align with another characteristic energy position, ϕ_0, caused by the surface states inside the band gap of the semiconductor. The dependence of ϕ_B and ϕ_m is thus weakened and can be described by the index S= $d\phi_B / d\phi_m$. Hence, ϕ_B is expressed as [3]:

$$\phi_B = S(\phi_m - \chi) + (1 - S)(E_g - \phi_0) \qquad (8.1)$$

where χ and E_g represent the electron affinity and the bandgap of the bulk semiconductor, respectively. In general, II-VI semiconductors have S > 0.5 (closed to ideal Schottky limit), while the values for silicon and III-V semiconductors are usually below 0.1 (severe Fermi level pinning) [3].

Various studies have been proposed to explain the presence of surface states (resulting in Fermi-level pinning) at the metal-semiconductor (MS) and insulator-

semiconductor (IS) interfaces. These models include the metal-induced gate state (MIGS) model [4], the unified defect model (UDM) [5-6], and the disorder-induced gap state (DIGS) model [7]. The core idea of the MIGS model is that the surface states are caused by the penetration of the metal wavefunction into the semiconductor. However, MIGS cannot explain why the Fermi level is pinned at the same energy level for both MS and IS interfaces. On the other hand, Spicer et al. points out that the Fermi level pinning of the III-V semiconductor is due to extrinsic defects, because the intrinsic surface states are already swept out of the band gap due to the rearrangement of the atoms near the surface after the epitaixal growth or wafer cleaving [5-6]. Spicer's data indicate that the Fermi level pinning position is insensitive to the species of adatoms, doping, and the crystal orientation of the III-V substrate. This implies that the formation of surface states is dominated by the near-surface crystalline defects created by the absorption of adatoms. The UDM model suggests that those incoming adatoms break the stoichiometric ratio of the surface III-V semiconductor, either with the local lattice disorder created by the absorption of oxygen atoms or the heat of adsorption of metal atoms on the surface of the semiconductor. The non-ideal stoichiometric ratio creates anti-sites at the surface, and therefore generates one acceptor level and one donor level in the bandgap. Figure 8.1 (a) shows the location of the Fermi level pinning described by UDM model. For the p-type InP used in our work, the Fermi level is pinned at between 0.1 eV and 0.3 eV below the conduction band minimum due to the exposure to oxygen [6].

Besides Spicer's work, Hasegawa, et al. showed that the surface Fermi level of the major tetrahedral semiconductors are coincidently pinned at the approximate position of -5.0 eV from the vacuum level [7]. Figure 8.1 (b) shows the measured interface state

distributions of common III-V semiconductors with various dielectric species on these surfaces [7]. The energies of the Fermi level pinning in these data are slightly different from Spicer's measurement. The DIGS model is then proposed to explain these results by considering the variation of bond length and angle due to the disordered surface semiconductor layer created during the adsorption of adatoms. In general, the DIGS model states that the degree of surface disorder determines the density of interface states, and thus how firm the Fermi level is pinned at the surface. Although there is some discrepancy between the UDM and DIGS models, the prediction of Fermi level pinning has to consider many factors, including the crystal anti-sites, vacancies, and surface disorder suggested by both models.

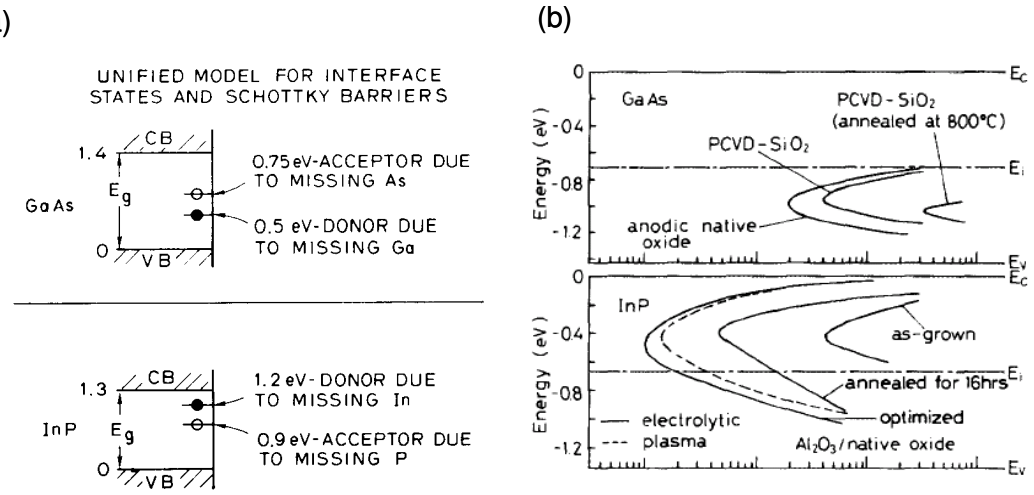

Fig. 8.1 *(a) The position of level pinning suggested by UDM model [5]*
(b) Measured surface state distribution of various IS interface [7]

The Fermi level pinning position of InP makes it a good candidate to provide a large Schottky barrier height if a p-doped substrate is used. A higher Schottky barrier height will allow for a larger quasi Fermi-level splitting when the solar cell is under illumination, and therefore accounts for the high open circuit voltage (V_{oc}) in Coutts'

work [1]. The conventional metal-insulator-model (MIS) is proposed to describe the behavior of the Schottky-type InP solar cell by assuming the existence of an interfacial layer of P_2O_5 between the InP substrate and the ITO contact [8]. However, Tsai, et al. found that the ITO/InP junction exhibits similar V_{oc} and spectral response compared to sputtered-Au/InP devices, but differs from that of thermally evaporated-Au/InP [9].The analysis from Hall measurements implied the existence of an n^+ layer at the surface of a sputter-etched, p-doped InP substrate [9]. Tsai, et al. therefore, speculate that the ITO/InP solar cell is in fact a buried p-n^+ homojunction at which the n^+ surface conducting layer is formed by phosphorus deficiency created during ITO sputtering. This hypothesis is confirmed by Luo, et al. by showing a higher Schottky barrier height of ITO/p-InP (~1.1 eV) than evaporated-Au/p-InP (~0.78 eV) [10]. As described by Shannon, the induced n+ layer near the p-InP surface provides the opposite space charge, and therefore increases the barrier height of ITO/p-InP [11]. Besides the case of ITO/InP, Luo, et al. point out that the common phenomena of sputter-induced of changes of the Schottky barrier height are also observed for Si, GaAs, and GaP [12]. The qualitatively energy band diagram of the ITO/InP device is shown in Fig 8.2 [10], and the influence of the induced n+ layer by sputtering can be seen by comparing the band profiles of these junctions.

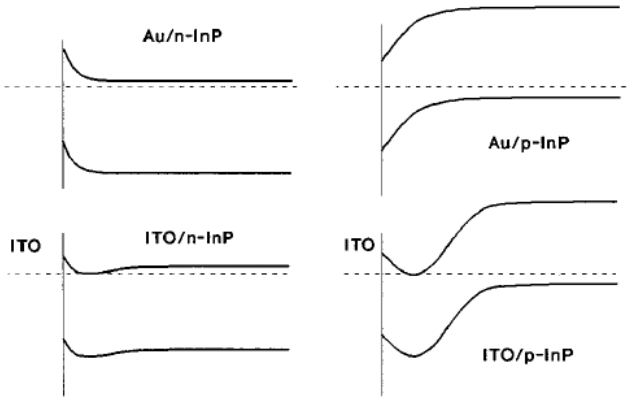

Fig. 8.2 *Energy band diagram of evaporated-Au/InP v.s. sputtered-ITO/InP[10]*

8.3 Cold welding

An important aspect of the fabrication process for thin-film solar cells described here is to efficiently bond III-V wafers onto the foreign substrate. In general, "bonding" means that when two atomically flat solids are brought in contact, both will stick to each other either with van der Waals forces, hydrogen bonds, or chemical bonds such as metallic, ionic, or covalent [13]. In this work, we utilize the formation of metallic bonding between two metal contact layers on InP and Kapton sheets to adhere the InP wafer onto the Kapton sheet. Since such metallic bonding can occur at room temperature, this kind of bonding is also called cold welding [14-15]. The fundamental principle of cold welding is based on a phenomenon called adhesive avalanche, namely, the sudden elimination of the interface between two clean, flat metal surfaces when the separation of both metals is comparable to the bulk interatomic distance [16]. In general, cold-welding occurs at room temperature and under air ambient. However, to strengthen the adhesion, it usually requires applying pressure (on the order of MPa) to overcome obstacles from the oxidized metal surface, contamination of dust particles, and hydrocarbons [13-14].

The noble metals are usually selected for cold welding due to their softness and chemical inertness to the atmosphere. In this work, the procedure of cold-welding starts from depositing Au layers on both InP wafer and plastic substrate. The method of deposition can be either evaporation or sputtering, as long as the resulting Au layer has no tensile stress, which causes poor adhesion to the substrate [17-20]. Both gold-coated samples are then quickly transferred to the stamping machine, which sits in a normal laboratory environment (greater than class 10,000), and are pressed face-to-face. The stamping pressure needs to be sufficient to overcome the dust particles on the interface,

but is also limited to the mechanical strength of the InP wafer. For this work, the typical stamping pressure to achieve cold welding is approximately 50M Pa.

8.4 Selective wet etching

Another important aspect of the fabrication process is to perform selective wet etching to remove the original InP substrate after cold-welding the entire epilayer plus substrate onto the plastic sheet. Typically, the wet etching process of a III-V semiconductor is characterized by its rate, anisotropy, and material selectivity, the latter of which is defined as the ratio of the etching rate between the target layer and the etch stop layer. For our work, etching anisotropy can be neglected as the etching takes place on the entire un-patterned substrate. Table 8.1 is a summary of wet etching systems for common III-V compound semiconductors [21]. In general, HF attacks oxides and high aluminum-content material such as AlAs or AlSb, while most of the indium or gallium-based compounds are immune to HF. HCl usually only targets phosphorus-based III-V materials such as InP, InGaP, and InAlP, and sometimes can combine with a weak acid such as H_3PO_4 to adjust its etch anisotropy [21]. For most arsenic-based III-V compounds, wet etching depends on the oxidation-reduction reaction at the wafer surface. This etching system typically consists of a mixture of H_2O_2 and another acid. H_2O_2 is responsible for oxidizing the III-V surface, while the newly-formed oxide layer is then quickly removed by the complementary acid. For $In_{0.53}Ga_{0.47}As$, the most commonly chosen acid is either citric acid [22] or H_2SO_4 [23]. Table 8.2 compares the characteristics of the etching rate of $In_{0.53}Ga_{0.47}As$ and the selectivity with respect to InP for both wet

etchant system [22-23]. It is found that citric acid/ H_2O_2 has better selectivity while H_2SO_4/ H_2O_2 exhibits higher etching speed.

Stopping layer	Sacrificial layer	Etchant
GaAs	$Al_xGa_{1-x}As$, $x \geq 0.5$	$HF:H_2O$
	$Al_{0.5}In_{0.5}P$	$HCl:H_2O$
	$In_{0.5}Ga_{0.5}P$	$HCl:H_2O$
	$Al_{0.5}Ga_{0.5}P$	$HF:H_2O$
$Al_xGa_{1-x}As$, $x \geq 0.40$	GaAs	$NH_4OH:H_2O_2$
$Al_{0.3}Ga_{0.7}As$	GaAs	succinic acid: NH_4OH
	GaAs	$C_6H_8O_7 : H_2O_2 : H_2O$
	$In_{0.2}Ga_{0.8}As$	$C_6H_8O_7 : H_2O_2 : H_2O$
AlAs	$In_{0.53}Ga_{0.47}As$	succinic acid: NH_4OH
	$In_{0.53}Al_{0.47}As$	d:o
InP	$In_{0.53}Ga_{0.47}As$	$FeCl_3:H_2O$
		$C_6H_8O_7 : H_2O_2 : H_2O$
	$In_{0.53}Al_{0.47}As$	$C_6H_8O_7 : H_2O_2 : H_2O$
	GaAs	$C_6H_8O_7 : H_2O_2 : H_2O$
	$Al_{0.3}Ga_{0.7}As$	$C_6H_8O_7 : H_2O_2 : H_2O$
	$In_{0.53}Ga_{0.47}As$	$HF:H_2OO_2:H_2O$
$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.13}Al_{0.34}As$,	$HCl:H_2O$
	$In_{0.53}Al_{0.47}As$	$HCl:H_2O$
	InP	$HCl:H_2O$

Table 8.1 *Illustration of selective etching for common III-V compounds [17]*

Etchant	Etch rate (μm/min)	Selectivity ($In_{0.53}Ga_{0.47}As$/InP)	Ref
$C_6H_8O_7:H_2O_2$ (7:1)	0.14	475	[18]
$H_2SO_4:H_2O_2:H_2O$ (1:1:10)	0.22	85	[19]

Table 8.2 *Comparison of etching characteristics of two etchant for selectively etch $In_{0.53}Ga_{0.47}As$ from InP [18-19]*

8.5 Fabrication and characterization of InP thin-film solar cells

The ITO/InP Schottky-type junction is chosen as the structure of the thin-film solar cell due to its simplicity of fabrication. The general fabrication procedure is to

combine techniques from Sec 8.3 and Sec 8.4 to bond the epi-grown InP wafer onto the Kapton substrate followed by sacrificially wet etching away the InP substrate which only leaves the epitaixial solar cell thin-film on the Kapton sheet.

The epitaxial solar cell structure is grown by gas source molecular beam epitaxy on a p-type, Zn-doped (100) InP substrate. The structure consists of a 0.375 μm thick, p-type ($5x10^{16}$ cm^{-3}) InP buffer layer, a 0.25 μm thick, a lattice-matched Be-doped ($5x10^{16}$ cm^{-3}) p-type $In_{0.53}Ga_{0.47}As$ etch-stop layer, a 2.0μm thick, lightly p-doped ($5x10^{16}$ cm^{-3}) InP base layer, and finally a 0.3 μm thick, lattice-matched Be-doped ($1x10^{19}$ cm^{-3}) p-type InP ohmic contact layer. The detailed growth condition is described at ref [10] of Chapter 2.

Figure 8.3 is an image and the fabrication procedure of InP thin-film solar cells achieved via substrate removal. The entire process starts with electron-beam evaporation of the p-metal contact with thickness of 300 Å Pt, followed by 300 Å Au on both the top InP contact layer and the 25 μm thick Kapton sheet. After metal deposition, the wafer is mounted metal-side down on the Pt/Au-coated plastic sheet. A bond is formed between the two metal surfaces via cold-welding [13-14] by applying a pressure of 50 MPa on an area of ~ $1cm^2$ for 60 s using an MTS Alliance RT/100 Testing System. The InP substrate and the subsequent $In_{0.53}Ga_{0.47}As$ etch-stop layer are then removed using a H_3PO_4: HCl = 1:3 solution, followed by H_2SO_4: H_2O_2: H_2O = 1: 1: 10. The etch rates for these solutions are 3 μm/min for InP and 0.2 μm/min for $In_{0.53}Ga_{0.47}As$, respectively. Finally, a 150 nm thick indium-tin-oxide (ITO) Schottky diode contact with the area of 0.785 mm^2 defined by a shadow mask is sputtered at a base pressure of $2x10^{-6}$ torr, RF power of 40 W, and deposition rate of 0.2 Å/sec. The sputtered ITO film typically has a resistivity of ~$1x10^{-2}$

Ω-cm and a transmission coefficient of ~80% to wavelengths in the range of 400 nm<λ< 900 nm [1, 24]. For comparison, a control ITO/InP solar cell with a structure similar to the thin-film device was similarly fabricated without substrate removal.

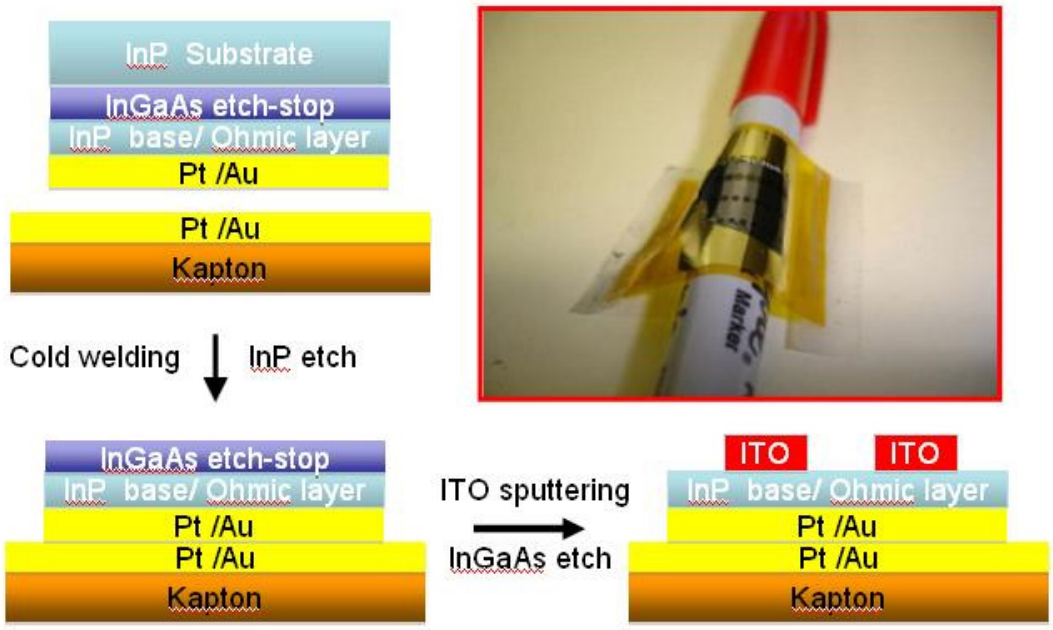

Fig. 8.3 Final i*mage and schematics of the fabrication procedure of thin-film ITO/p-InP solar cells*

The intensity-dependent current density (J) vs. voltage (V) characteristics were measured following the procedures described in Ch.5. Figure 8.4 shows the room temperature J-V characteristics of both thin-film and control photovoltaic cells under simulated AM1.5G solar spectrum at 1 sun intensity (100 mW/cm^2). From the dark *J-V* characteristics and its fit by generalized Schottky equation, shown at Fig. 8.5, of the thin-film device, the ideality factor of the thin film solar cell is estimated to be n=1.11, and the specific series and shunt resistances are 5.1 Ω-cm^2 and > 1 x 10^8 Ω-cm^2, respectively. The high specific series resistance originates from the highly resistive ITO contact and back metal contact, and is primarily responsible for the low fill factor of the solar cell.

The short circuit photocurrent density is J_{sc} =30±3 mA/cm^2, while for the control, J_{sc} = 24.9±2.5 mA/cm^2. Integration the measured EQE (see inset of Fig. 8.4) over the AM1.5 solar spectrum gives J_{sc} =25±3 mA/cm^2 and 20±2 mA/cm^2 for the thin-film and control cells, respectively, consistently indicating the same trend of the photoresponse between two solar cells. The ideal EQE response, shown in Fig 8.6, can be estimated based on the reflection at the InP/air interface and absorption by InP based on its optical properties [25] and those of gold [26]. Obviously, the absorption of photons reflected from the Au contact allows the thickness of the thin film solar cell to be further reduced. Nevertheless, this effect is not obvious for the ITO/p-InP device structure, since the heavily Zn-doped InP substrate contributes some photocurrent besides the lightly Be-doped InP epitaxial layer grown on top.

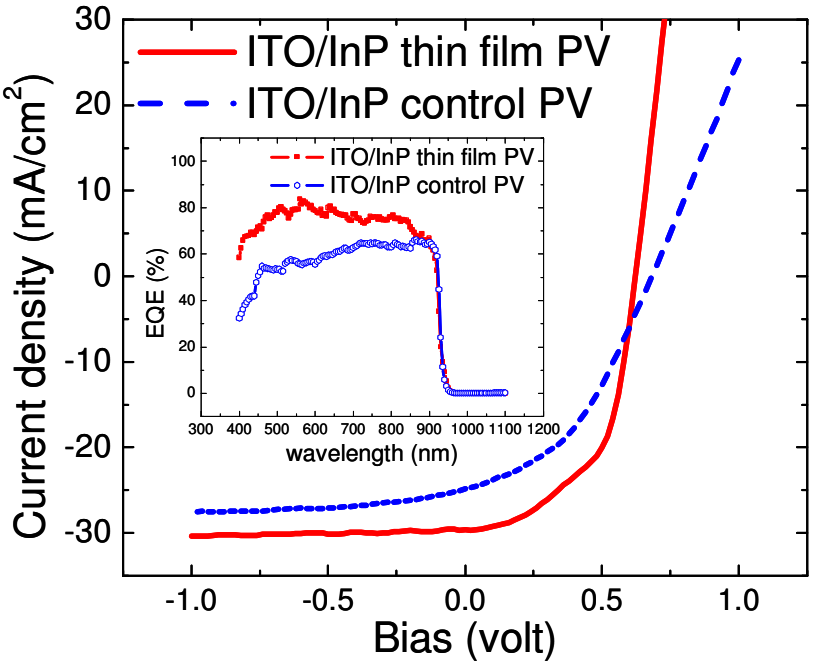

Fig. 8.4 *Current density versus voltage characteristics of the ITO/InP thin film and control solar cells under 1 sun, AM1.5G simulated solar illumination.* ***Inset****: External quantum efficiency as the function of wavelength of the ITO/InP thin film and control solar cells.*

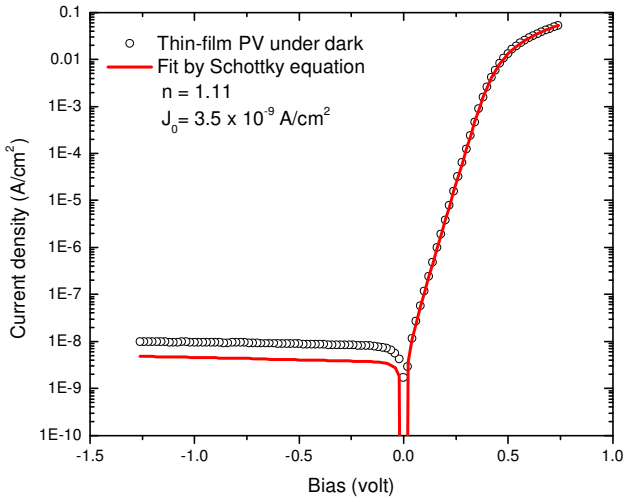

Fig. 8.5 *Current density versus voltage characteristics of the ITO/InP thin film and control solar cells under dark. The fit curve is based on generalize Schottky equation.*

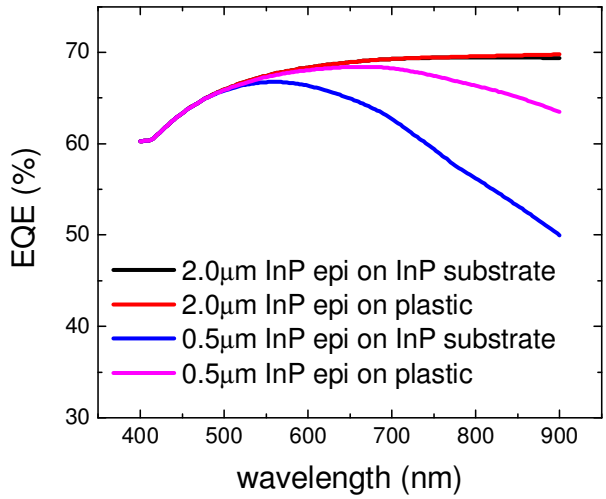

Fig. 8.6 *The calculated EQE response for both thin-film and conventional bulk cells with various thickness of InP base layer.*

Figures 8.7(a) and (b) show the V_{oc}, fill factor, J_{sc}, and η_p of the ITO/InP thin-film and control solar cells, respectively, as functions of simulated illumination intensity. The V_{oc} of the control solar cell is linearly proportional to the logarithm of the optical intensity, as expected for an intensity-independent responsivity. However, the thin-film solar cell V_{oc} is pinned for illumination intensities >0.5 suns. The reason needs to be

further investigated, but the pinned V_{oc} indicates that the thin-film devices suffers more carrier recombination, most likely due to the surface states from both the front ITO contact and the back metal contact as the illumination level increases. The fill factor of both devices decreases at high solar intensity because of the high specific series resistance. The lower shunt specific resistance of the control device further decreases the fill factor. Consequently, the power efficiency of the thin-film cell at one sun is η_p= 10.2±1.0% while the control has η_p=7.0±0.7%.

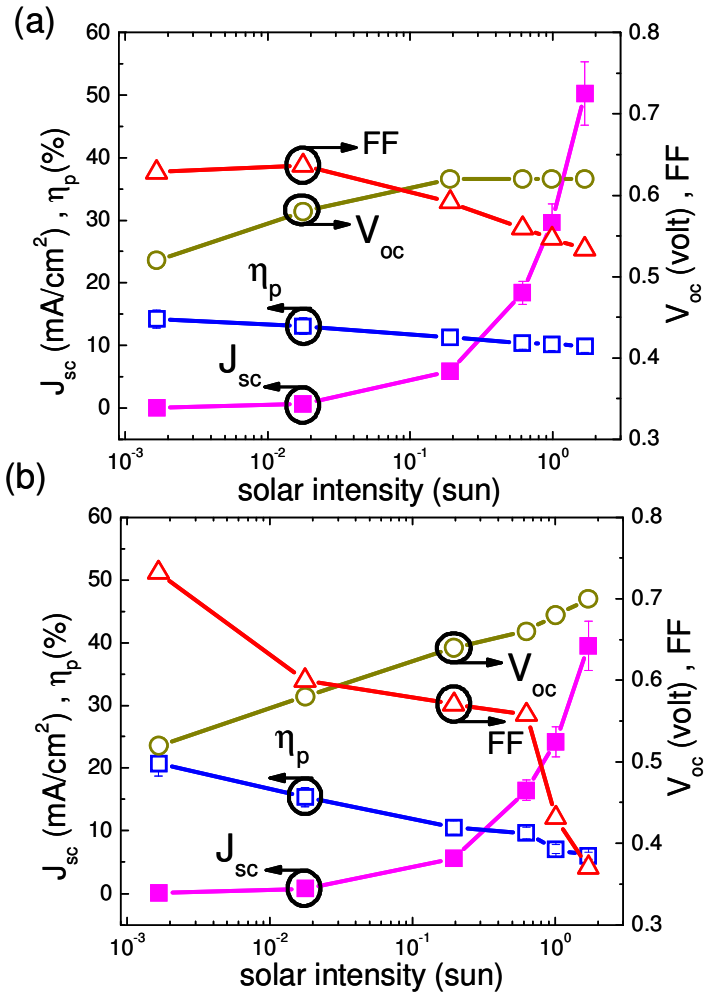

Fig. 8.7 *Open circuit voltage (V_{oc}), fill factor (FF), short circuit current (J_{sc}), and power conversion efficiency (η_p) as a function of illumination intensity under a AM1.5G simulated solar spectrum of the (a) thin film ITO/InP (b) control solar cell.*

The flexibility of the thin-film solar cells was tested by bending the devices either inward or outward over cylinders of various radii, as shown in the photo of Figure 8.8 (inset). Inward bending applies compressive strain, while outward bending results in tensile strain to the InP layer (see inset, Fig. 8.8). For each bending radius, the thin-film solar cell is stressed for 30s, released, and then characterized. Figure 8.8 shows J_{sc} and η_p, respectively, following the stress test. Here, η_p remains unchanged for inward bending radii > 0.5 cm (compressive strain ~ -0.097%), and for an outward bending radius > 1.0 cm (tensile strain ~ 0.049%). However, once stressed beyond these values, J_{sc} shows a decrease, leading to a concomitant reduction in power conversion efficiency. Figure 8.9 shows microscope images of typical thin-films on Kapton before and after experiencing tensile stress over a 0.3 cm radius. Before the stress test, the thin-film exhibits the "+" shape cracks due to the rough surface of the Kapton sheet. After the tensile stress test, the cell exhibits a large density of cracks that are parallel to the cylindrical axis, while the cell subjected to compressive stress shows no obvious damage. Although stress-induced cracks have an adverse impact on the solar cell performance, the stress tolerance of this InP thin film solar cell can be improved by using a thinner plastic sheet as the substrate, or placing the thin film at the neutral stress surface located at the center of a sandwich formed by two identically thin sheets of plastic [27]. Also, we note that ITO itself is brittle and subject to cracking during stress [28]. It is unclear whether the cracks initiate in the ITO and propagate into the InP, or vice versa.

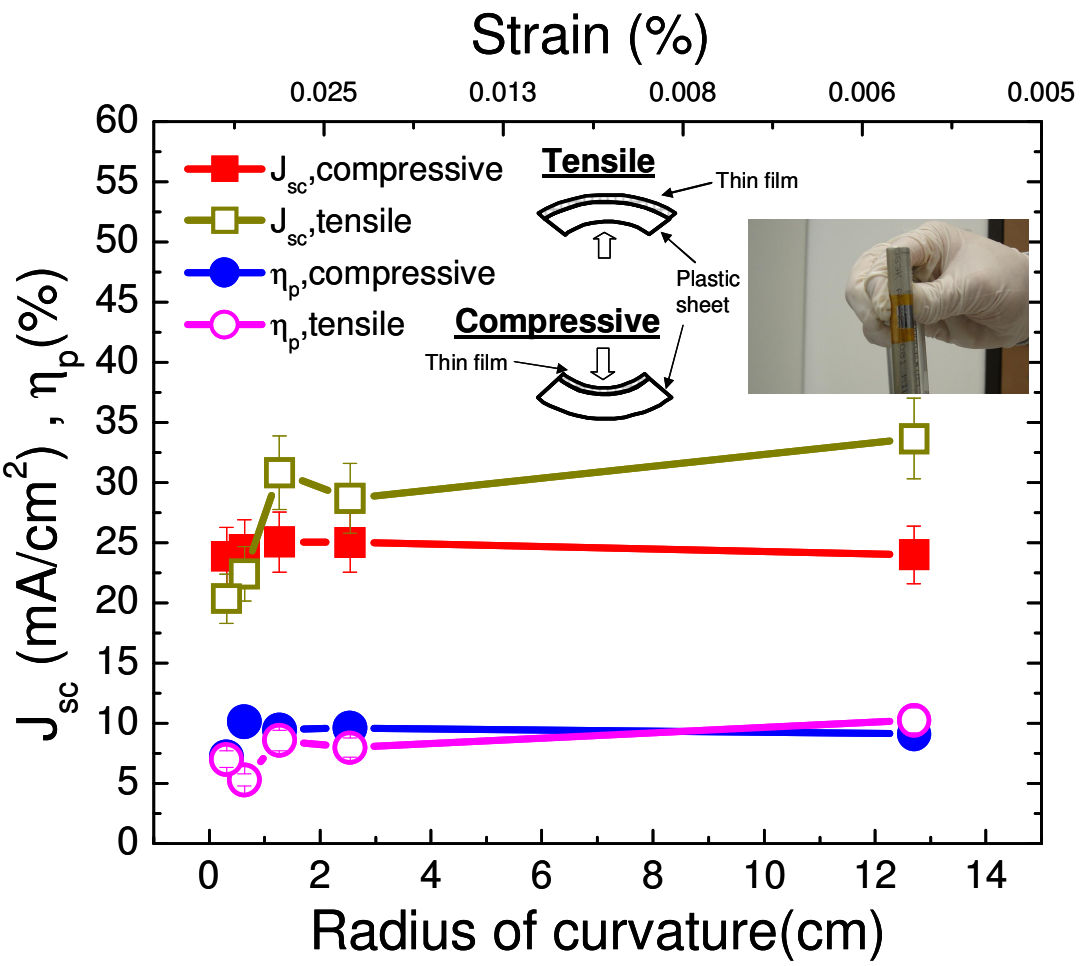

Fig. 8.8 *Short circuit current (J_{sc}) and power conversion efficiency (η_p) of the thin film ITO/InP solar cell after either the compressive (bending inward) or tensile (bending outward) stress test under 1 sun, AM1.5G simulated solar illumination.* ***Inset****: Diagram and image of the bending test.*

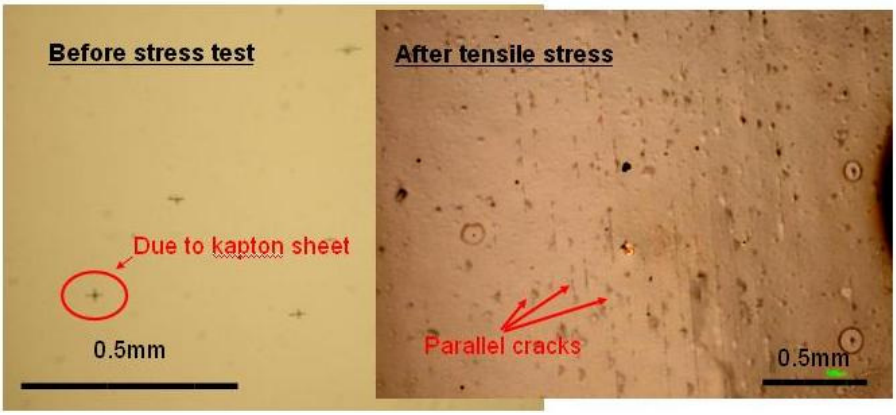

Fig 8.9 *Micrograph of thin-film before and after the tensile stress test*

Since the Kapton® has a significantly lower density (~ 1.42g/cm^3) than InP (4.81 g/cm^3), the thin-film solar cell is useful for applications where power conversion using lightweight devices is important [29-34]. Based on the device structure and the measured power efficiency, the specific powers of the thin-film and control ITO/InP solar cells are P_{sp}= 2.0±0.2 kW/kg and 0.041±0.004 kW/kg, respectively, while CIGS or CdTe thin-film solar cells have reported specific powers of 2.3 kW/kg [31] and 1.5 kW/kg [33], respectively, if the same thickness of plastic substrate is used. A detailed comparison of this work with other reported thin-film solar cell technologies is provided in Table 8.3. By adopting thinner plastic substrate and using higher efficiency solar cell architecture, over double the specific power is anticipated.

Table 8.3: Comparison of different thin-film solar cells on flexible substrates

	ITO/p-InP	CIGS	CdTe	GaAs
Substrate (Thickness)	Kapton foil 25 µm thick	Upilex foil 25 µm thick	Upilex foil 25 µm thick	Glass 75 µm thick
η_p (%)	10.2±1.0	14.1	11.4	19.2
P_{sp} (kW/kg)	2.0±0.2	2.3	1.5	1.1
V_{oc} at 1 sun (V)	0.62	0.649	0.765	1.0
J_{sc} at 1 sun (mA/cm^2)	29.6±2.9	31.5	20.9	31.8
Fill factor	0.55	0.69	0.71	0.806
Reference	This work	[31]	[33]	[34]

Note: The η_p of the CIGS cell is calculated by assuming that the density of CIGS film is 5.85g/cm^3, and the top metal contact consists of a 5µm thick Al/Ni stack with 5% device coverage [32].

8.6 Summary

In this chapter, we have demonstrated ultrathin-film InP Schottky-type solar cells bonded to flexible plastic substrates via cold-welding [35]. The device exhibits a power conversion efficiency of 10.2±1.0% and a specific power of 2.0±0.2 kW/kg. The devices are capable of withstanding either compressive or tensile strain by bending over radii of 1.0 cm or greater. This work provides an alternative method for adopting III-V semiconductor solar cells for portable, air and space-borne applications where very high specific power efficiency is required.

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Chapter 9

Cost reduction for InP thin-film solar cells by epitaxial lift-off

9.1 Introduction

In Ch. 8, we successfully demonstrated high performance of III-V thin-film solar cells bonded to plastic. That process sacrifices the entire III-V substrate to make a single thin-film type device. To further compete with the existing technologies of thin-film solar cells, it is necessary to lower the cost by re-using the original III-V seed substrate to make multiple III-V thin-film growths. This chapter will describe an ITO/p-InP thin-film solar cell with a power efficiency of 5% fabricated with an epitaxial lift-off (ELO) process, and demonstrate the re-usability of the original InP substrate for subsequent epitaxial regrowths and removals.

9.2 Overview of technology of re-using substrate for re-growth

III-V solar cells generally have superior power conversion efficiencies to their silicon counterparts. However, they cannot compete with silicon solar cells because of the notoriously high cost of the III-V substrate. Table 6.2 indicates that the production cost of thin-film type solar cell on an inexpensive substrate (e.g. a plastic sheet) is at least 10 times cheaper than a bulk solar cell. Hence, the evolution of solar cells from bulk to thin-film is an inevitable trend towards the scheme of lowering cost. Unlike silicon, there is still no effective way to directly grow single- or large grain poly-crystalline III-V thin-films on unconventional substrates, either by direct epitaxy or grain growth demonstrated

at Chapter 7. Therefore, one solution to achieve a low-cost III-V thin-film solar cell is to directly attach the III-V wafer with a grown solar cell epilayer on a foreign substrate, separate the grown epilayer from the III-V mother wafer, and reuse this original III-V seed substrate for the fabrication of subsequent III-V thin-film solar cells.

Techniques to separate the epi-layer from the mother substrate are hydrogen-induced exfoliation (ion-cutting) [1-4] and lift-off [5-8].The idea of ion-cutting is to intentionally create crystalline vacancies at the interface between the epitaxial thin-film and the mother substrate with ion-implanted hydrogen or helium ions, so that the subsequent thermal annealing can establish the build-up H_2 or He pressure inside these vacancies to exfoliate the thin-film from the substrate. Figure 9.1 is a schematic of the ion-cutting process to make a silicon-on-insulator (SOI) structure [1]. The ion-cutting process has been successful for application to Si-based structures. Recently, this technique has been duplicated on III-V materials [3-4]. However, unlike Si, the challenge is that the implanted hydrogen/hellium ions may have very different interaction with group-III atoms versus group-V elements. The resulting stoichiometric damage cannot be easily cured by thermal annealing [2] and impacts the electric behavior of the thin-film devices [4].

Besides the newly emerging ion-cutting technology, ELO is another technique that utilizes chemically selective wet etching of a sacrificial layer to separate the epitaxial thin-film from the mother substrate [5]. Figure 9.2 illustrates the concept of ELO [5]. The epi-layer, consisting of stack of GaAs and low-aluminum-content AlGaAs, is separated

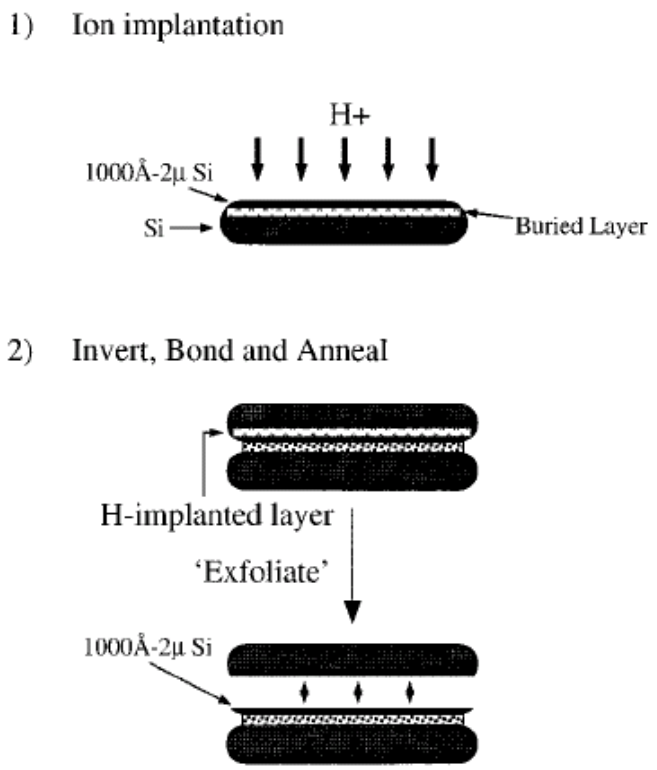

Fig. 9.1 *Schematics of the process of hydrogen-induced exfoliation (ion-cut) [1]*

from the GaAs substrate with the undercut removal of a sacrificial AlAs layer. Since HF has more than 10^7 selectivity between AlAs and GaAs [5], the undercut of AlAs eventually releases the epi-layer from the GaAs substrate by immersing the entire sample into dilute HF. The critical step of ELO is to efficiently vent the chemical reactant of AlAs and HF, consisting of H_2, AsH_3, and AlF_3 [5-6], so that fresh HF molecules can keep reacting with the exposed AlAs. To expedite the out-diffusion of chemical reactants, Fig. 9.2 shows the usage of the tension from black wax to curl the epitaxial thin-film from the GaAs substrate as the undercut of AlAs proceeds. This allows the ELO to be completed within hours for the wafer size of a few centimeters. Currently, high efficiency (26.1%) GaAs homojunction thin-film solar cell ELO on a glass substrate has been

demonstrated [7]. There is still no direct example to prove the re-usability of the original mother substrate after ELO. In this chapter, we will show progress in fabrication of ITO/p-InP thin-film solar cell made by ELO, and the feasibility of re-using the original parent InP wafer.

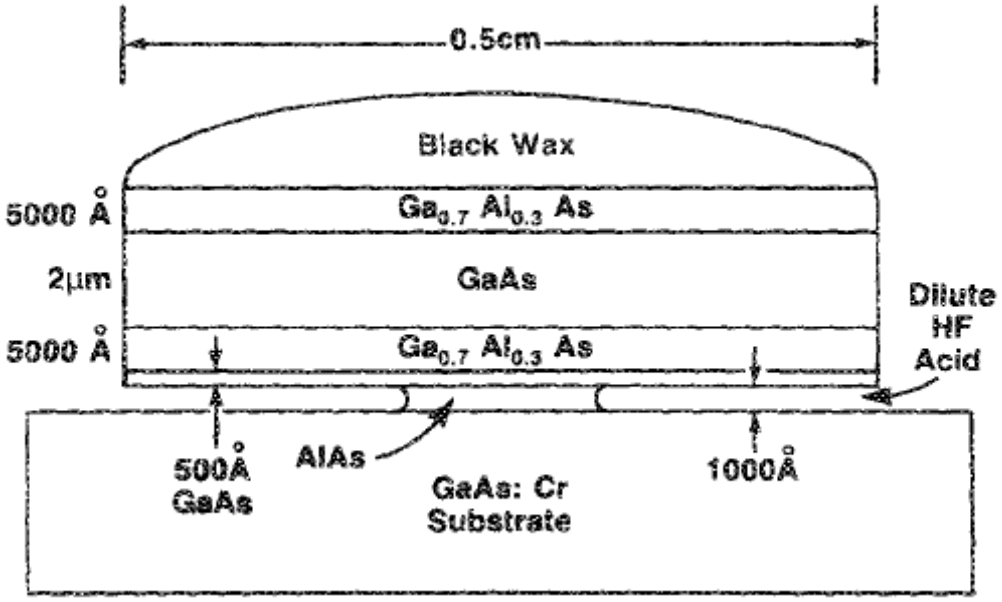

Fig. 9.2 *Demonstration of ELO at the material system of AlAs/GaAs [5]*

9.3 Surface pretreatment for wafer re-growth

In this work, we will combine the techniques of cold-welding and ELO to demonstrate III-V thin-film solar cell on plastic substrate and the reusability of the original III-V substrate. The selected solar cell structure is ITO/InP Schottky junction due to its ease of fabrication, while the AlAs sacrificial layer, inserted between InP base layer and InP substrate, is the sacrificial layer for ELO. The important requirement of this process flow is to ensure the re-usability of the InP wafer after the ELO process has been employed to remove the original thin-film InP epilayers. Ideally, any epi-grown wafer

after exposure to air can follow the original epitaxial procedure to re-grow new layers on its surface. However, moisture, oxygen or impurities from air will degrade the quality of the wafer surface, subsequently lowering the quality of the re-grown layer by introducing carrier depletion or accumulation at the re-grown layer/original substrate interface [9]. Ingrey found that the Auger spectra of the fresh InP surface in air suffers much stronger signals from carbon and oxygen than the one originally covered with oxide [10]. They imply that the hydrocarbon contaminants accumulate much faster on a fresh III-V surface than on an oxidized surface, emphasizing the importance of preparing high quality of native oxide on the wafer surface prior to epitaxial re-growth. UV/ozone is the widely accepted technique [9-12] to re-grow a native oxide, as this process removes hydrocarbon contaminants on the wafer surface, and provides a reproducible and stoichiometric native oxide [9-10]. Typically, a native oxide layer of around 1 nm thickness is suitable to encapsulate the surface from air contaminants, and can be easily thermally desorbed during re-growth. Besides UV/ozone, another alternative is through wet chemicals to clean the hydrocarbons and the air-induced native oxides, and form a new passivation layer. One example is to use HF to form an H-terminated surface that is widely used to reduce the surface recombination velocity of silicon or GaAs [10, 13]. On the other hand, sulfidation treatment by $(NH_4)_xS$ can form a stable S-InP surface for re-growth [9]. However, it is likely that the sulfur atoms at the sulfidized-surface will become n-type donors after the re-growth, leading to local charge accumulation.

9.4 Fabrication and characterization of InP thin-film solar cell made by ELO

Figure 9.3 (a) is a schematic of the apparatus used for the ELO process. The epitaxial-ready wafer, cold-welded onto a plastic sheet, is mounted on a Teflon rod with radius R (~ 3.8cm). The teflon rod is then immersed into dilute HF solution (HF: H_2O=1:10) with an external force applied on one side of the wafer. With the progress of the undercut of the sacrificial layer, the photovoltaic thin-film is gradually bent at the curvature of R, therefore expediting the out-diffusion of the chemical reactant between dilute HF and the sacrificial layer. Figure 9.3 (b) is the image of the wafer mounted on the Teflon rod ready for the ELO process. Here, the external force is gravity applied by a silicon rod mounted on the III-V wafer via wax. Figure 9.3 (c) is a photo of a final InP thin-film on a plastic sheet after ELO using this apparatus.

The epitaxial solar cell structure, grown by gas source molecular beam epitaxy on a p-type, Zn-doped (100) InP substrate, consists of two parts – one is a stack of protection layers, and the other is the photovoltaic layer itself. The protection layers, consisting of an $In_{0.53}Ga_{0.47}As$ layer of 0.2μm thick and an InP layer with 2.0μm thick, are used to prevent the degradation of the surface of the InP mother substrate in HF solution during ELO. The photovoltaic layer is comprised of a 0.5μm thick $In_{0.53}Ga_{0.47}As$ layer, lightly p-doped ($3x10^{16}$ cm^{-3}) 1.2μm thick InP base layer, and a 0.3 μm thick, Be-doped ($2x10^{18}$ cm^{-3}) p-type InP Ohmic contact layer. The $In_{0.53}Ga_{0.47}As$ layer is used to protect the InP base layer from the slow attack of dilute HF during ELO. Here, a 20nm thick layer of AlAs is inserted between the protection layers and photovoltaic layer to serve as the sacrificial layer. The details of the structure are shown in Table 9.1.

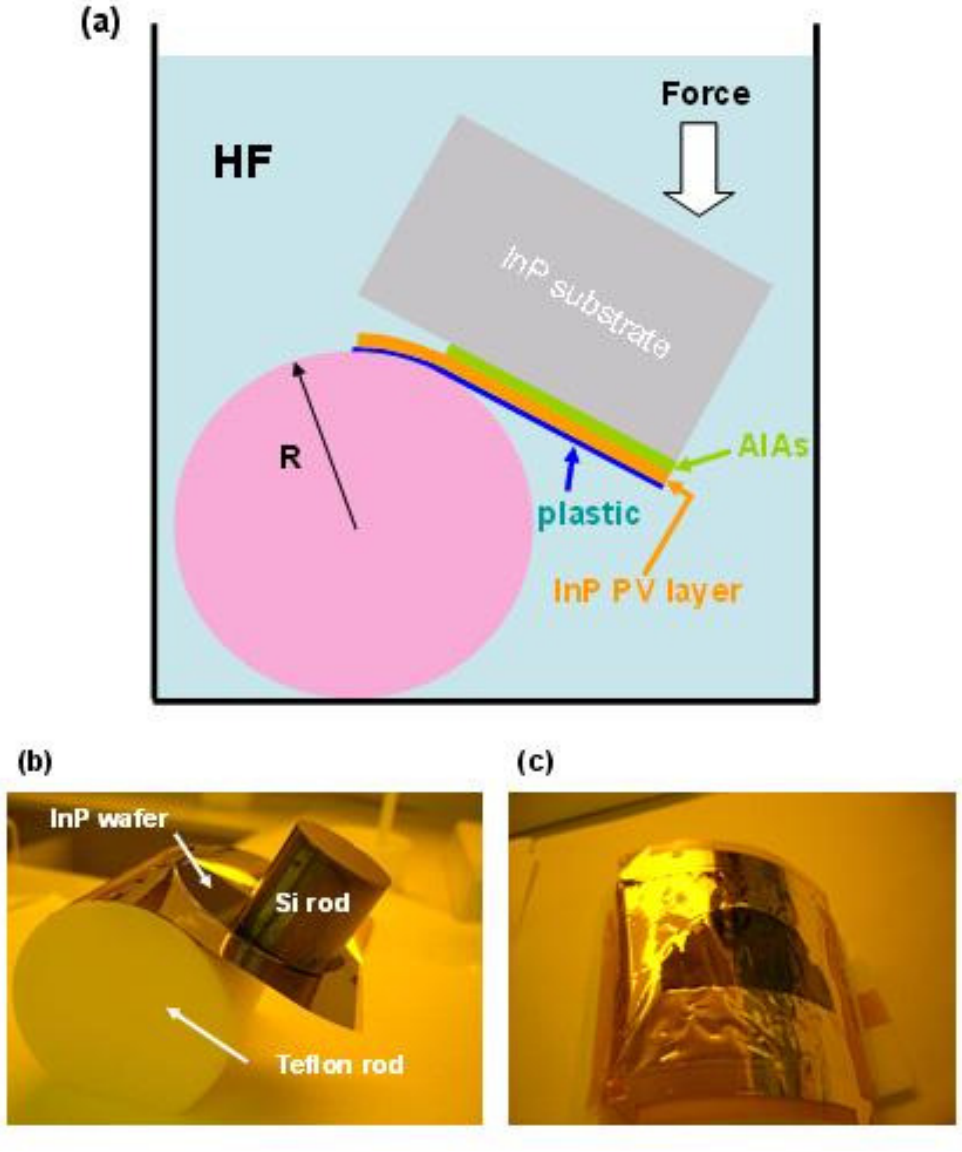

Fig. 9.3 *(a) Schematics of the apparatus for ELO process (b) The photo of the mounting of the wafer ready for ELO (c) The photo of the InP thin-film on plastic sheet after ELO*

Material	Thickness	Doping	Function
InP	350μm	Zn $3x10^{17}cm^{-3}$	Substrate
InP	0.5μm	Be $3x10^{17}cm^{-3}$	p-type buffer
$In_{0.53}Ga_{0.47}As$	0.2μm	Be $3x10^{17}cm^{-3}$	Protection layer
InP	2.0μm	Be $3x10^{16}cm^{-3}$	Protection layer
AlAs	10nm	Be $3x10^{16}cm^{-3}$	Sacrificial layer
$In_{0.53}Ga_{0.47}As$	0.5μm	Be $3x10^{16}cm^{-3}$	Protection layer
InP	1.2μm	Be $3x10^{16}cm^{-3}$	Base
InP	0.3μm	Be $2x10^{18}cm^{-3}$	P-contact

Table 9.1 *Epitaxial layer structure of the thin-film photovoltaic for ELO process (The detailed growth condition is described at ref [10] of Chapter 2)*

The device fabrication process starts with sputtering of the metal contact to a thickness of 600 Å Au on both the top InP contact layer and the 75 μm thick polyvinylidene fluoride (PVDF) sheet. After metal deposition, the wafer is mounted metal-side down on the Au-coated PVDF sheet and a bond is formed between the two metal surfaces via cold-welding. After cold-welding, a silicon rod with weight of 8 gram is mounted on the back side of the cold-welded InP substrate via wax. The entire assembly is attached to a Teflon rod with radius of 7.5 cm via kapton tape, and then immersed into dilute HF (HF: H_2O = 1:10). After taking 10 days to complete ELO, both the photovoltaic thin-film on PVDF and the mother InP substrate are rinsed in de-ionized (D.I.) water for 10 mins. Figure 9.4 is the schematic and photographs of the thin-film on PVDF and mother substrate after the D.I. water rinse. The Au residue on the mother

wafer is due to the local incomplete ELO. Also, the partial cloudy area at the surface of the thin-film indicates damage to $In_{0.53}Ga_{0.47}As$ caused by the HF solution. We speculate that 10 days of ELO may dissolve the $In_{0.53}Ga_{0.47}As$ protection layer and attack the InP thin-film underneath.

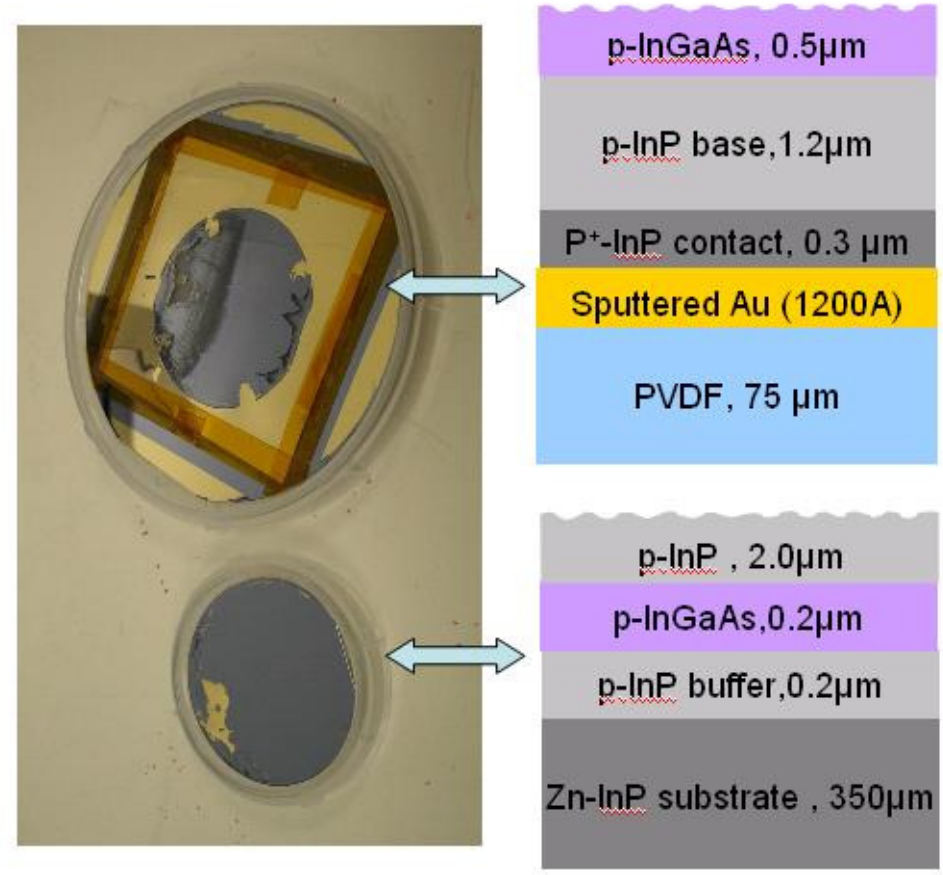

Fig. 9.4 *Photos and schematics of the InP thin-film and the mother substrate after the ELO process*

This mother InP substrate is then dipped into TFA etchant (provided by Transene Inc.) to totally remove the gold residue. Then, the InP and $In_{0.53}Ga_{0.47}As$ protection layers are selectively removed with solutions of H_3PO_4: HCl = 1:3 and H_2SO_4: H_2O_2: H_2O = 1: 1: 10, respectively. The exposed fresh InP substrate surface is then degreased with hot trichloroethylene, acetone, and hot iso-propanol followed by intentional growth of native

oxide with UV/ozone for 10 mins. This cleaned mother substrate is then loaded in the MBE for the re-growth of the second photovoltaic epitaxial layer. The layer structure of the epitaxial re-growth consists of Be-doped ($2x10^{18}$ cm^{-3}) 0.5 μm thick InP buffer layer and a lightly Be-doped ($3x10^{16}$ cm^{-3}) 1.2 μm thick InP base layer separated by a Be-doped ($2x10^{18}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$ layer. This $In_{0.53}Ga_{0.47}As$ layer serves as the etch-stop layer to ensure that the re-grown solar cell has the same lightly p-type base layer thickness as the previous ELO thin-film solar cell. The appearance of 2x and 4x RHEED patterns, shown in Fig 9.5, after growing the first 15nm thick InP buffer layer implies flatness of the mother substrate after the chemical pre-treatment. After the re-growth, the side contact is defined with selective InP wet-etching, evaporating Zn/Au of 200 Å /2000 Å, and thermal annealing at 410^0C, for 1 min under N2 ambient. Finally, a 100 nm thick indium-tin-oxide (ITO) Schottky diode contact with the area of 0.014 cm^2 defined by a shadow mask is sputtered at a base pressure of $6x10^{-7}$ Torr, an RF power of 70 W, and deposition rate of 0.4 Å/sec. Figure 9.6 shows the image of the thin-film solar cells, and the schematics of the final device structure of both thin-film and re-grown solar cells.

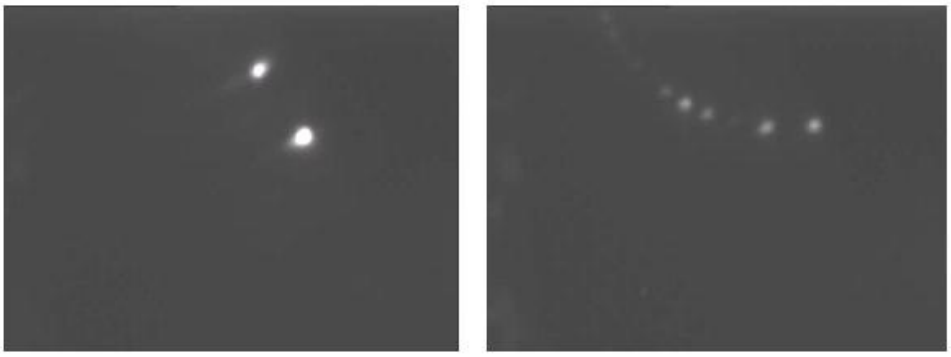

Fig. 9.5 *The RHEED pattern after the growth of 15nm InP buffer layer on the Chemical pre-cleanned mother InP substrate*

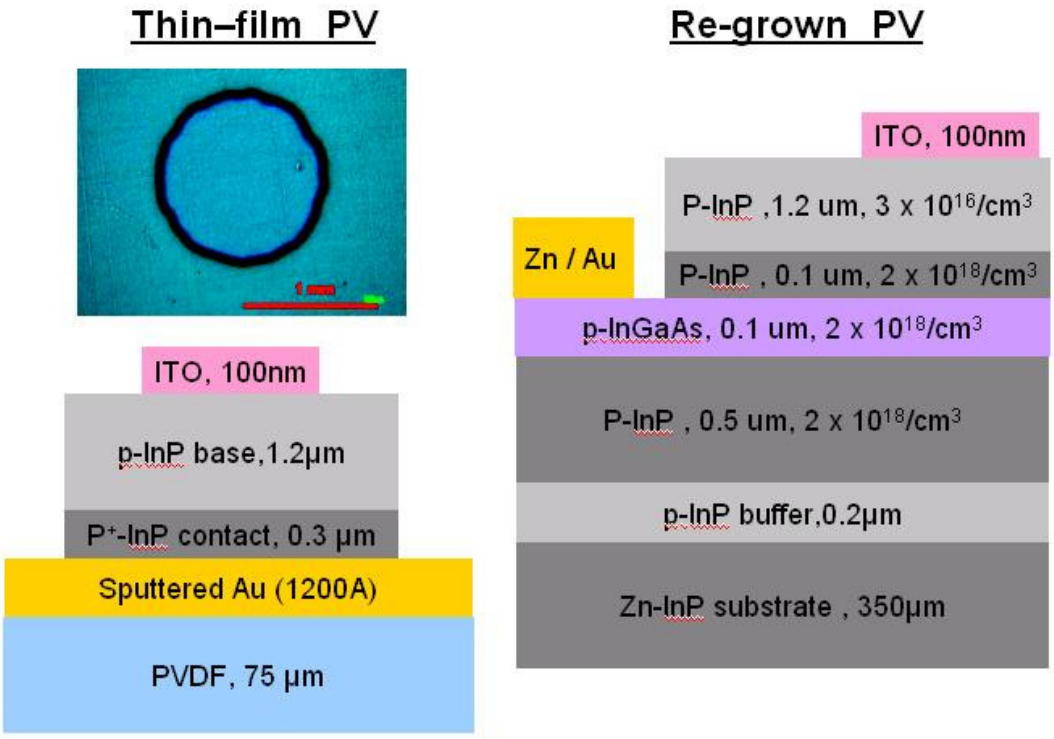

Fig. 9.6 *The micrograph of the thin-film solar cell and schematics of the final device structure of both thin-film and re-grown solar cell*

To understand the intrinsic impact of ELO process on the re-growth of the mother substrate, a control cell is grown and fabricated under the simulated condition of the ideal ELO process. Here, the same two protection layers ($In_{0.53}Ga_{0.47}As$ and InP) are grown on fresh iron-doped InP substrate by GSMBE. After growth, this wafer is dipped in dilute HF (HF: H_2O = 1:10) for 46 hrs. Following the same procedure of surface pretreatment, the control solar cell with a similar epitaxial structure is re-grown and fabricated as the ELO structure described above. The ITO contact of the control cell is sputtered with a lower power of only 40W, and at a slower deposition rate, 0.2 Å/sec. Figure 9.7 illustrates the schematic of the device structure of the control cell.

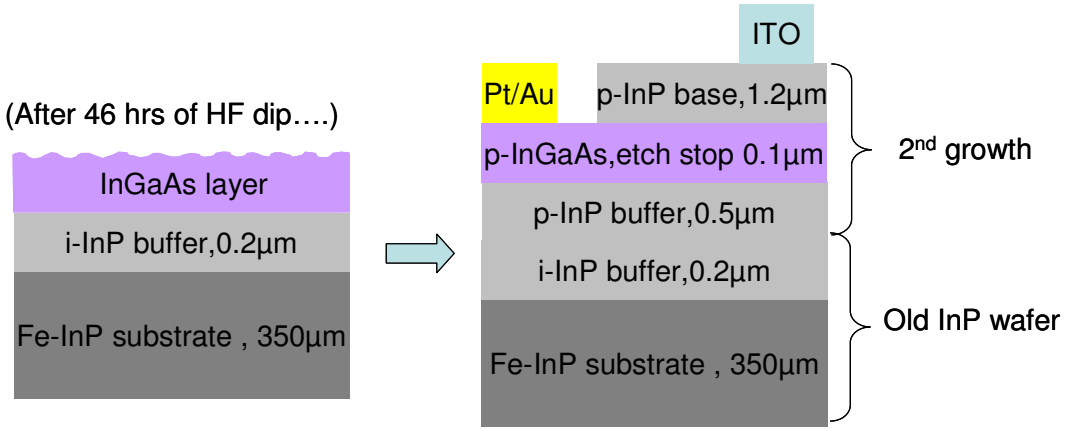

Fig. 9.7 *The schematics of control cell fabricated under the ideal ELO condition.*

The performance of these solar cells is characterized by following the same procedure described in Ch. 6. Figure 9.8 is the J-V characteristics of each cell under both dark and simulated AM1.5G solar spectrum at 1 sun intensity. The specific series resistance, reverse saturation current, and ideality factor are fit with the generalized Schottky equation described in Ch.6. Apparently, both the thin-film and re-grown cell (sputtered ITO with 70W) have significantly higher leakage currents, reverse saturation currents and ideality factors than the control cell (sputtered ITO at 40W). The sputtering process can create donor-like defects that result in a thin n^+ (10^{19} cm^{-3}) layer at the surface of InP substrate [13-14]. These defects can either assists carrier tunneling [14], resulting in higher reverse saturation/leakage current, or enhance the non-radiative recombination rate in the space charge region, causing a higher ideality factor. The comparison between these solar cells is consistent with previous work ([1] at Ch.8) that emphasizes the importance of reducing substrate damage by ensuring lower power and deposition rate for ITO sputtering.

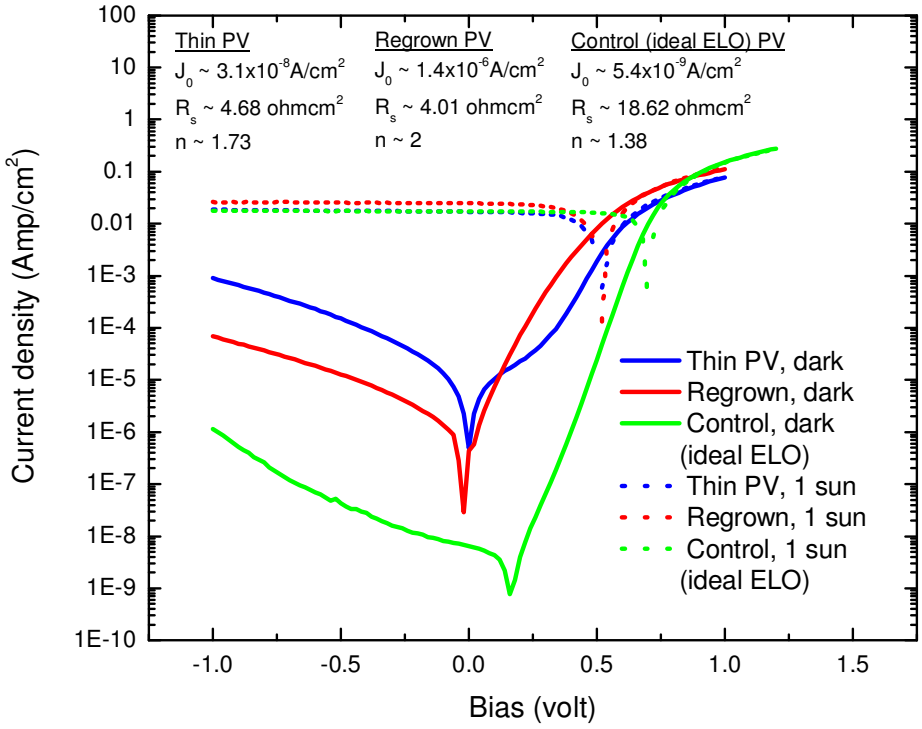

Fig. 9.8 *J-V characteristics of the thin-film cell, re-grown cell, and the control cell under both dark and simulated AM1.5G solar spectrum at 1 sun intensity.*

Figures 9.9 (a)-(d) show the J_{sc}, V_{oc}, fill factors, and power conversion efficiencies of each solar cell as functions of simulated illumination intensity. In general, J_{sc} is linearly dependent on the illumination intensity. The higher J_{sc} of the re-grown cell than the remaining two cells is possibly due to the additional contribution of the photocurrent from the Zn-doped InP substrate. Nevertheless, the re-grown cell exhibits lower V_{oc} than the control cell because it has higher reverse saturation current, possibly induced by high RF power during ITO sputtering. For the thin-film cell, the V_{oc} is pinned at illumination intensities >0.5 suns, suggesting that the Schottky barrier height may be lower than for the other two cells. Beside the use of high ITO sputtering power, there are two other possibilities that could be responsible for the lower V_{oc} of the thin-film cell:

1. The slow chemical attack from dilute HF (~10 days) changes the type of the surface defects on the thin-film surface, and therefore alters the energy levels of the defects located in the bandgap.
2. The metal sputtering process induces a thin n^+ layer at the InP surface [13]. Figure 9.10 is the schematic and band profile of the cells under illumination with either evaporated or sputtered Au as the back contact. As indicated in Fig 8.10, this n^+ layer may induce a larger Schottky barrier at the back side of the thin-film, and therefore give the local quasi-Fermi level a larger energy range over which it can swing under illumination. The cancellation of quasi-Fermi-level splitting between both front and back interfaces reduces the readout of V_{oc}.

The solution to the first problem is to reduce the time of the ELO process by improving the design of ELO apparatus, while the second can be mitigated by replacing Au sputtering with Au evaporation for the back side metal contact of the wafer. The fill factor of the control cell is higher than for the other two cells due to its two orders of magnitude lower leakage current, equivalent to higher specific shunt resistance. However, the fill factor decreases at high solar intensity because of the high specific series resistance. Consequently, the power efficiency of the thin-film cell, re-grown cell, and control cell at one sun are approximately 5.0%, 7.0%, and 8.5%, respectively.

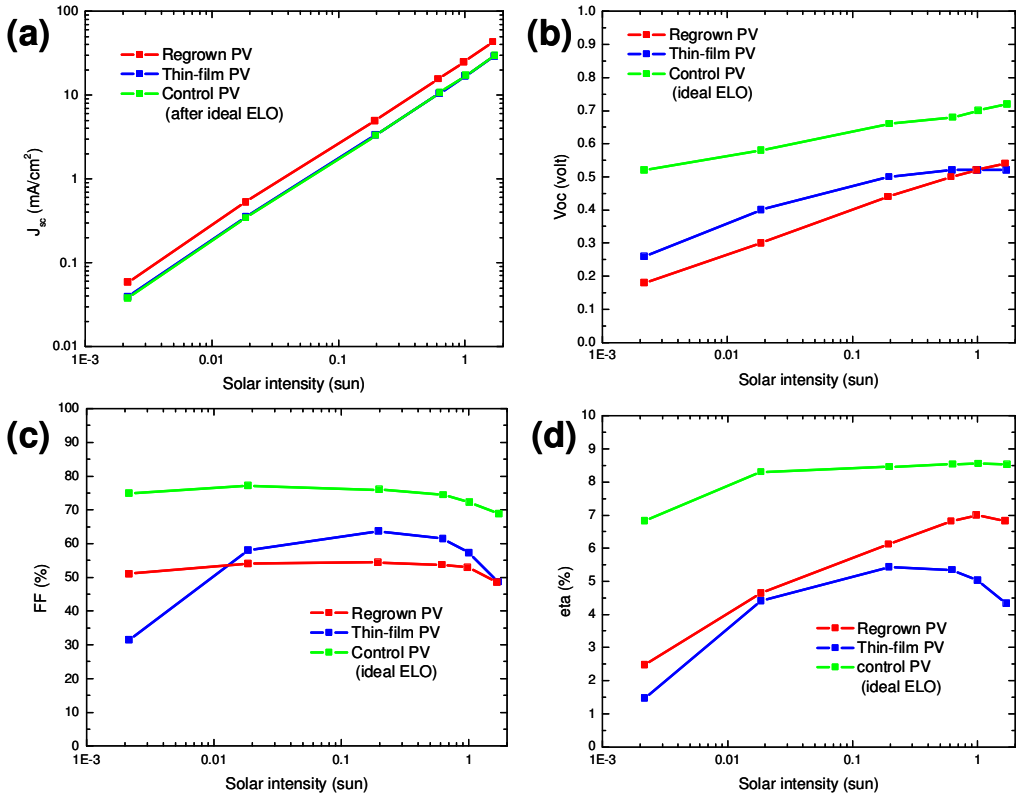

Fig. 9.9 (a) J_{sc}, (b)V_{oc}, (c) fill factor, and (d) power conversion efficiency (eta) of the thin-film cell, re-grown cell, and control cell as the function of simulated illumination intensity.

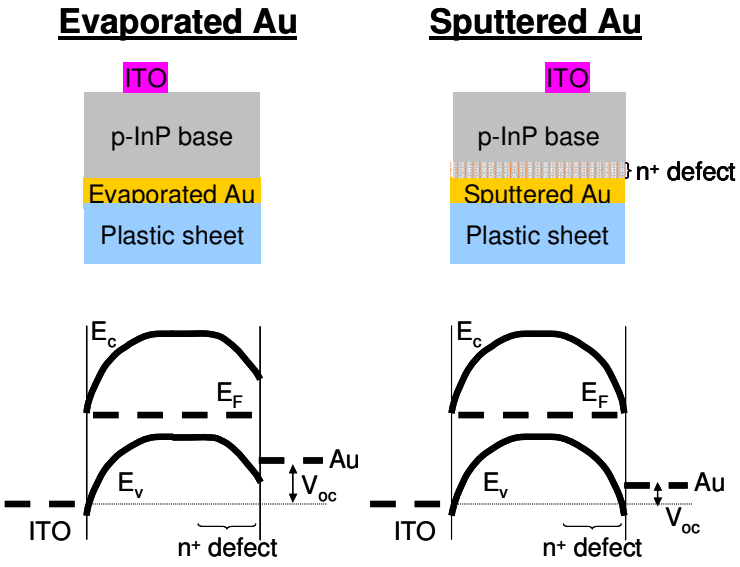

Fig. 9.10 *The possible profile of the thin-film solar cell under illumination with either evaporated-gold or sputtered-gold as the back contact.*

9.5 Anticipated improvements

To speed up ELO, it is necessary to modify the apparatus shown in Fig 9.3(a). Here, the angle between the wafer surface and the direction of external applied force is initially 90^0 before ELO. As ELO proceeds, the wafer continues to peel off from the plastic, which reduces this angle and therefore lowers the torque from the external applied force. This means the speed of ELO keeps dropping as ELO continues. To fix this problem, it is necessary to dynamically rotate the Teflon rod so that the angle between the wafer surface and the external force always is at 90^0. Figure 9.11 shows the schematic and photo of the modified apparatus for ELO. Compared to Fig. 9.3(a), this apparatus allows the user to manually adjust the rotation of the Teflon rod during ELO. With this new feature, the time required to finish the ELO of the entire 2-inch InP wafer drastically reduces from 10 days to 48 hours. It is expected that the ELO time can be further reduced by utilizing motors to automatically maintain the angle between wafer and external applied force during the entire ELO process.

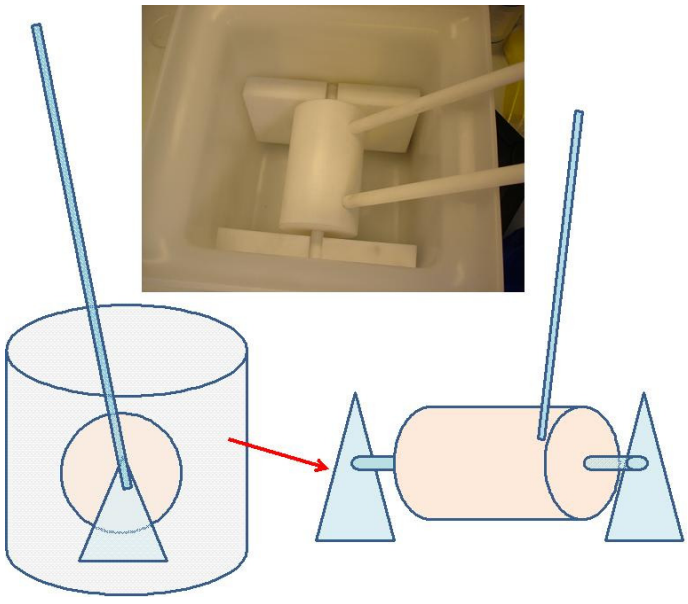

Fig. 9.11 *The schematics and photo of the modified apparatus of ELO process*

Besides expediting ELO process, another improvement is to adopt InP/InGaAs epitaxial layers to protect the solar cell thin-film from HF during ELO. It is expected that the ELO process can create thin-film solar cell that has the same performance as its bulk counterpart [7]. Nevertheless, in this work, the tensile stress from AlAs sacrificial layer will inevitably introduce crystal dislocations in the InP base layer. It is shown that polycrystalline GaAs cell grown on polycrystalline Ge ([21] at Ch.7) substrate has a lower efficiency (~18%) than the single-crystalline GaAs cell (~26%) [7]. Hence, it is reasonable to speculate that the optimal efficiency ITO/InP thin-film solar cell produced by ELO may lie within the range of 15% ~ 19% at 1 sun intensity.

9.6 Summary

In this chapter, we have proven the concept of fabricating an InP thin-film solar cell by the ELO process while maintaining the re-usability of the original mother substrate. The entire ELO takes 10 days to complete with current design of the ELO apparatus. The performance of the thin-film, re-grown, and control cells have been characterized and compared. In general, the control cell has a lower ideality factor and leakage current than the other two cells due to its low ITO sputtering power. The ITO sputtering power, Au cathode sputtering process, and HF attack may be responsible for low V_{oc} of the thin-film cell. In short, the ELO process exhibits the feasibility for realizing inexpensive III-V thin-film solar cells by demonstrating the power efficiency of 5% for ITO/p-InP thin-film and 7% for re-grown solar cell.

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Chapter 10

Conclusions and future work

10.1 Part I – Integrated Photonics

Chapter 2, we applied the Mach-Zehnder interferometer architecture to demonstrate a current-driven, 2x2 optical switch based on the InP-InGaAsP material system. The optical switch exhibits contrast ratio of (21±2) dB for both TE and TM polarizations over the wavelength range from λ=1520nm to 1580nm. Also, a five-channel AWG is fabricated with the same material system, and shows an insertion loss of 12±2dB, a channel non-uniformity of 2dB, and a crosstalk between channels of -15±2dB.

In Ch. 3, we successfully demonstrated a monolithically integrated optical receiver (SOA-PIN) for light generation/detection in a reconfigurable-optical-add-drop-multiplexer (ROADM) circuit. The SOA and PIN shares the same multiple quantum well structure, and the light is coupled through asymmetric twin-waveguide (ATG)-tapers between the SOA and P-I-N detector. This integrated receiver exhibits a peak external responsivity of 8.2±0.4 A/W, and a 3 dB bandwidth of 11±1 GHz, corresponding to an internal gain-bandwidth product of 265±35 GHz.

The entire ROADM circuit is assembled and shown in Ch. 4 using the passive and active components in Ch. 2 and Ch. 3. The total chip size is 6mm x 10mm, and the add-drop functionality is verified through add and drop ports of the circuit. Despite the successful proof-of-concept demonstration of lightwave processing by the ROADM circuit, to further spread this concept to market readiness, the first priority is to overcome the high insertion loss and crosstalk shown in this ROADM circuit. The AWG used is

primarily responsible for both issues. In theory, reducing the gap between arrayed waveguide at the free propagation region can reduce the loss and crosstalk which requires further optimization of the fabrication of the AWG by adopting projection lithography, use of appropriate photoresists, and dry etching.

To go beyond the scope of photonic integration, in Chapter 5, we collaborate with IBM T.J. Watson Research Center to demonstrate InP-based enhancement mode MOSFETs. Here, the buried channel structure is adopted to mitigate the issue of surface Fermi-level pinning. The resulting long channel MOSFET has a peak transconductance of 42 mS/mm, while that of the short channel device is 157 mS/mm. The sub-threshold slope is affected by D_{it} and therefore ranges between 150 and 200 mV/decade. The successful demonstration of the enhancement mode MOSFET shows the potential to have high speed electronics fully integrated with complex photonic integrated systems.

10.2 Part II - Thin-film solar cells

This part of thesis work demonstrated thin-film III-V solar cells on inexpensive plastic substrates. In Ch. 7, we demonstrate the direct growth of GaAs thin-films on quartz substrates. The growth procedure consists of the defining GaAs seed layers followed by the grain growth done with high temperature selective epitaxy. The resulting size of the GaAs clusters is approximately 700nm, while X-ray diffraction indicates that the grain size is ~ 100nm. To be comparable to single-crystalline solar cell, the polycrystalline grain size has to be on the order of millimeters. This will require significant amount of growth time, and make direct growth an uneconomical approach for mass production of III-V thin-film cells.

Chapter 8 demonstrated the feasibility of having III-V thin-film epitaxial solar cell based upon MBE-grown InP materials. By adopting cold-welding and InP substrate removal, the ITO/p-InP thin-film solar cell exhibits a power conversion efficiency of 10.2±1.0% and a specific power of 2.0±0.2 kW/kg. The stress test also indicates that this cell is capable of withstanding either compressive or tensile strain by bending over radii ≤ 1.0 cm without degradation. This demonstration provides an alternative method for adopting III-V semiconductor solar cells for portable, air and space-borne applications where very high specific power efficiency is required.

Chapter 9 continues the work to further reduce the production cost of InP thin-film solar cells. By adopting the ELO process, both the fabrication of thin-film solar cells, and preservation of the original mother substrate are achieved. The same mother substrate is then re-grown with same solar cell layer structure. The resulting thin-film, re-grown, and control solar cell exhibits the efficiency of 5.0%, 7.0%, and 8.5%, respectively.

Future work on III-V thin-film solar cells should concentrate on optimizing the process of direct bonding with ELO. Efforts should be focused on improving the design of current ELO apparatus to increase the speed of the process. The next generation design of the apparatus should be capable of dynamically rotating the Teflon rod during the ELO process. In this way, the external applied force can keep supplying maximum torque on the wafer to speed up the curl of the thin-film, and therefore reduce the time to finish the ELO. Based on the cost analysis at Ch 6, the projected cost of thin-film cells with well-developed ELO process together with current available III-V wafer technology is close to $2.0/Wp. Although this is still more expensive than a-Si, CdTe or CIGS cell, it is capable of competing with conventional single-crystalline silicon bulk cells. In other words, ELO

will allow for terrestrial applications and mobile vehicles to be equipped with high efficiency III-V cells competitive with current silicon bulk cell. Furthermore, III-V thin-film solar cells can possibly continue to compete with a-Si, CdTe or CIGS cells if the III-V industry continues to develop large size (> 6-inch) III-V wafers and the corresponding processing equipment to reduce the material cost of thin-film and mother substrate.