A High Voltage High Power (HiVP) Class-E Power Amplifier at VHF

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***Abstract* — A four stage cascoded class-E power amplifier based on a high voltage / high power technique (HiVP) technique has been designed and implemented. The amplifier is fabricated using four separate flanged LDMOS transistors. Drain voltage has been reduced to increase the maximum frequency of class-E operation mode and to reduce the maximum drain voltage swing to protect the transistor from breakdown. Measurement results show 69% power-added efficiency (PAE), 30.1 dB of gain and 51.8 W output power at 150 MHz.**

***Index Terms* — Aluminum Oxide, class-E, high voltage /high power (HiVP), power amplifiers, thermal management of electronics.**

I. Introduction

Systems operating at VHF such as synthetic aperture radars (SAR) and radio broadcasting require a large amount of RF power. At these power levels, thermal management becomes a critical design issue. Hence, designing a high efficiency power amplifier is required to reduce the amount of heat dissipation. Furthermore, high efficiency designs improve power amplifier reliability.

Switching mode power amplifiers (class-D, class-E and class-F) are often used to design high efficiency power amplifiers at VHF [1], [2], [3]. Class-D power amplifiers are able to provide the highest output power for a given drain voltage. However, their efficiency starts to drop as the frequency increases beyond the HF range. Class-F power amplifiers require an output circuit that provides short or open at harmonic frequencies which is difficult to implement at VHF or lower frequency ranges [3],[4]. On the other hand, class-E power amplifiers provide an attractive solution due to their high efficiency and ease of implementation.

The gain and the output power of a power amplifier are limited by the device technology. For VHF based SAR systems, where the output power has to be more than 1 kW, it is almost impossible to achieve such a power levels with high efficiency using a single transistor. To overcome this limitation, the output power from several power amplifiers can be combined together. Traditional power combining approaches often result in increased size and design complexity for the PA [5], [6]. HiVP is an alternative way to combine the power from several transistors. This approach has been demonstrated using monolithic circuit techniques [7] - [12]. The main advantage of HiVP is that its optimum output impedance is increased as the number of transistors increases while facilitating impedance matching to 50 ohms. Such a design allows the power amplifier to have wider bandwidth and lower matching losses.

Designing hybrid HiVP power amplifiers using packaged devices is challenging because the transistors' source has to be connected to the drain of the adjacent transistors (cascode topology). In discrete high power transistors, the source terminal is connected to the device flange to be mounted on a heatsink. This complicates the implementation of HiVP configuration using packaged devices. In this paper, four BLF571 LDMOS devices have been power combined using the HiVP amplifier design. A new hybrid circuit level implementation of the HiVP technique has been addressed in.

II. Circuit Design

The first step in the design of HiVP is to select the drain supply voltage for a single transistor (V_{ds1}). The maximum drain to source voltage that can be reached in class-E power amplifier is V_{max} where [2]:

$$V_{max} = 3.647\ V_{ds} \tag{1}$$

The transistor chosen for this work has a V_{max} of 110V. Hence, V_{ds1} has been selected to be 25 V in this design. After designing the single class-E power amplifier, the HiVP class-E power amplifier with four transistors can be designed as shown in Fig. 1. Assuming that Z_{opt} is the optimum impedance at the drain of the first transistor, the optimum impedance at the drain of the second, third and fourth transistors are $2Z_{opt}$, $3Z_{opt}$ and $4Z_{opt}$ respectively. Hence, the values of C_2, C_3 and C_4 have to be selected to provide the best inter stage matching between each two transistors which can be approximated from the following relation [7]:

$$Z_{source\_n} = \frac{1}{gm}\frac{(C_{gs} + C_n)}{C_n} \tag{2}$$

Where Z_{source_n} is the source impedance of the nth transistor [7].

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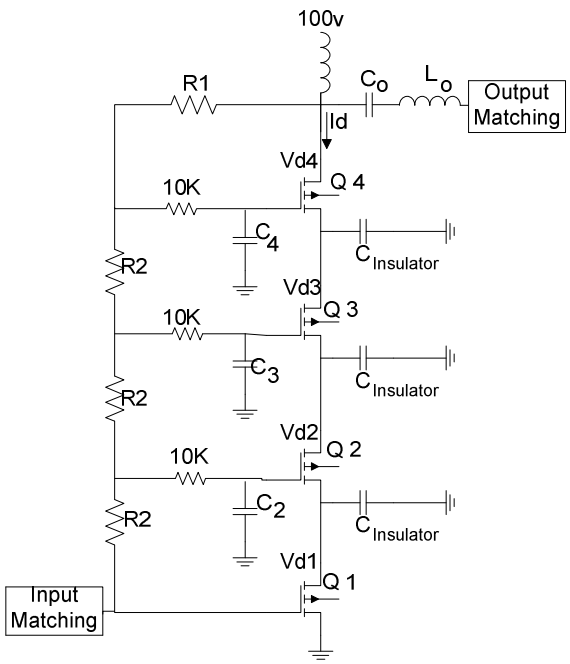

Fig. 1. Circuit Schematic of HiVP class-E power amplifier.

A detailed diagram of the device interconnection is shown in Fig. 2. Since transistor source cannot be accessed directly (the source is connected to a flange for heatsinking), the source of each transistor is connected to the drain of the adjacent transistor via a copper tape as shown in Fig. 2. The entire structure is mounted on a heatsink. In order to insulate the transistor sources from each other, 1.52 mm thick alumina insulators are placed between the heatsink and the transistor flanges. Alumina has been selected here as an electrical insulator because of its low thermal resistance. The parasitic capacitance introduced through AL_2O_3 insulator to ground ($C_{Insulator}$) has been modeled using HFSS, and determined to be approximately 8 pF. The impact of $C_{Insulator}$ on the design of inter stage matching between the transistors has been taken into account. Although the effect of $C_{Insulator}$ is minimal, slight tuning of the circuit allows one to compensate for its effects.

The copper tape connecting sources to drains is modeled as a microstrip transmission line with alumina substrate. Hence, there is a small phase shift between the drain voltages of the adjacent devices. A photo of the fabricated power amplified is shown in Fig. 3.

Other alternative replacements to the Aluminum Oxide insulator with high thermal conductivity are Mica, Beryllium Oxide, Aluminum Nitride and Diamond but each have drawbacks that make them unattractive for this circuit implementation.

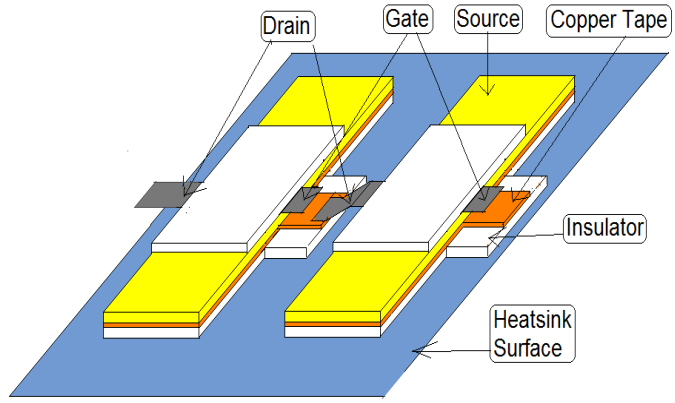

Fig. 2. Multiple packaged cascode connection.

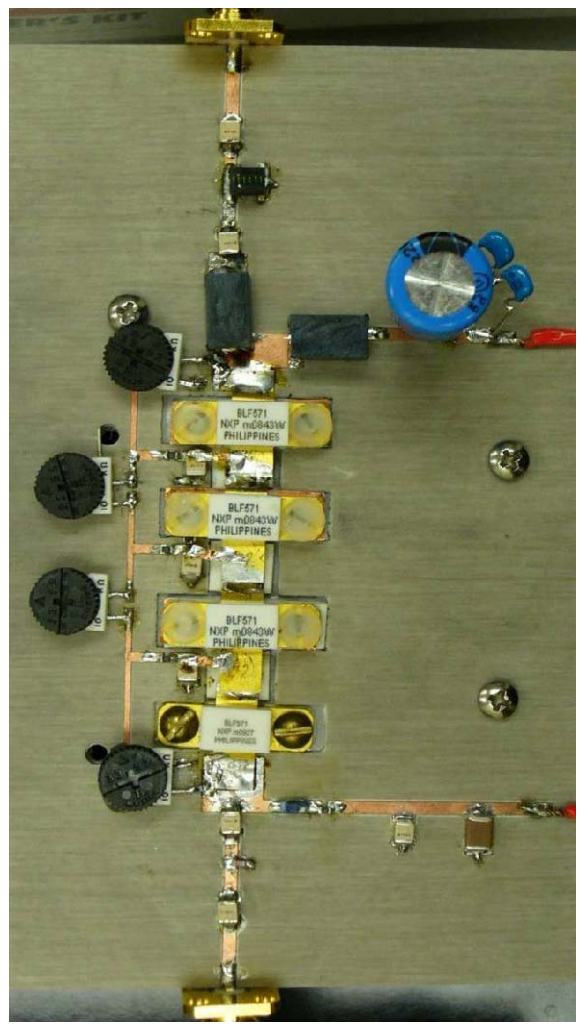

Fig. 3. Fabricated HiVP Class-E power amplifier.

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III. Simulation and Measurement Results

The Advanced Design System (ADS) software has been used here to simulate the performance of the power amplifier. The time domain waveforms of the drain voltage (Vd4) and the drain current (Id4) of Q4 has been simulated as shown in Fig. 4. The DC value Vd4 is 100 V which is divided across all of the four transistors. It can also be noticed that Id4 is almost zero when the Vd4 reaches its maximum value which indicates that the amplifier is operating in class-E mode. Voltages and currents at the drain of Q1, Q2 and Q3 show similar waveforms with lower voltages levels.

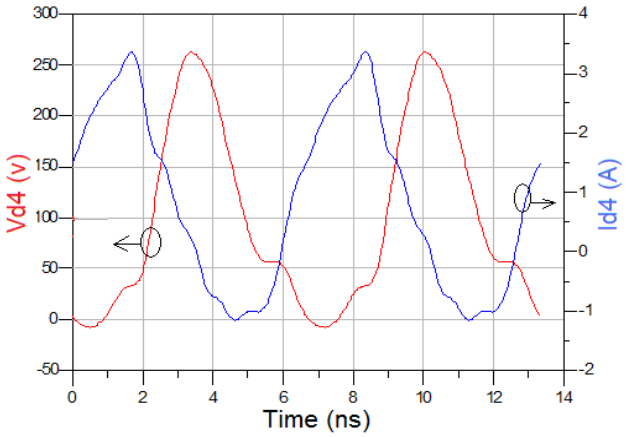

Fig. 4. Simulated drain voltage and drain current waveforms.

The power amplifier was designed at the center frequency of 150 MHz. Its simulated results show an expected gain of 31.2 dB, PAE of 82 % and 69 W output power at 150 MHz. Its measured gain, power added efficiency and output power at 150 MHz are 30.1 dB, 69 % and 51.8 W respectively. The measured 1 dB bandwidth is 20 MHz. Comparison between the simulated and measured gain, PAE and output power versus frequency at 17 dBm input power is shown in Fig. 5. The discrepancy between the measured and the simulated results can be due to several factors including device model inaccuracy, device parameter variations, as well as small delays between the drain current of the adjacent devices that have not been fully compensated for.

It can be noticed from Fig. 5 that the highest gain achieved is 30.77 dB at 140 MHz with 59.9 W output power and 63% PAE. In order to find the maximum achievable output power, the amplifier has been tested with different input power levels at 140 MHz. Plots of the simulated and measured output versus input power at 140 MHz are provided in Fig. 6. The highest measured output power level is 65.4 W with a PAE of 63.5%.

Essentially by cascoding four devices, not only power combining has been achieved but also the overall PA's gain has been improved by four times as compared to a single device. In addition to that, impedance matching to 50 ohms is facilitated thereby reducing the output matching losses.

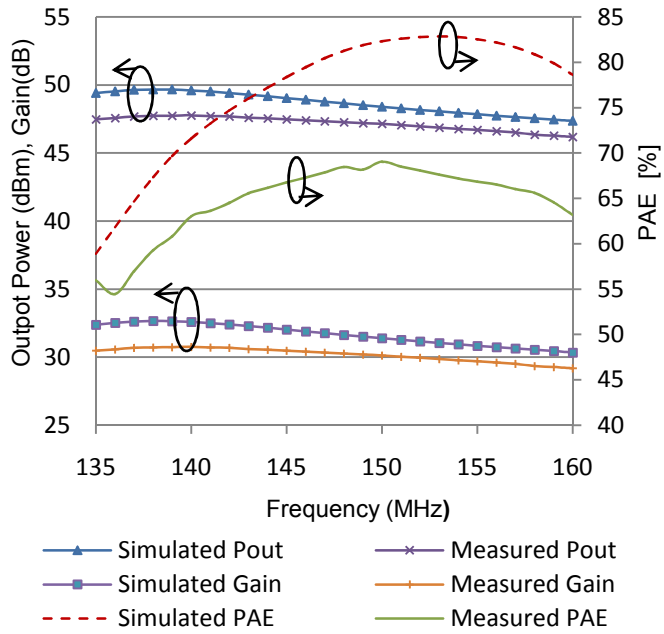

Fig. 5. Measured and Simulated PAE, output power and power gain versus frequency at 17 dBm input power.

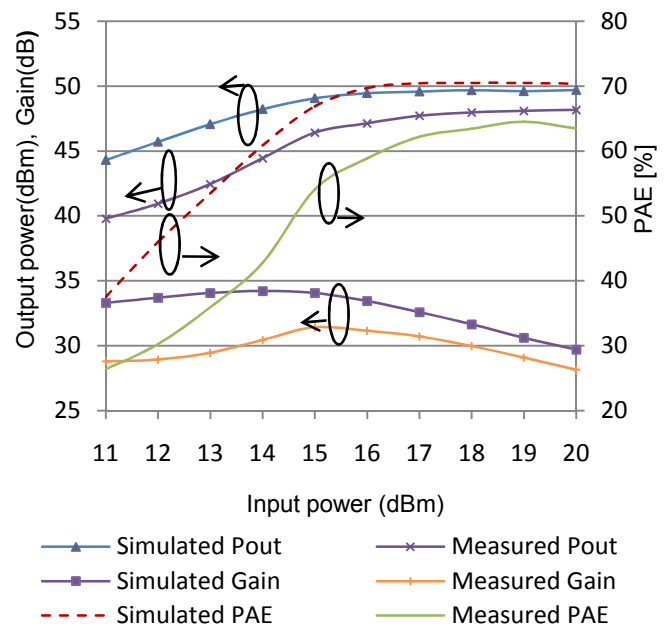

Fig. 6. Measured and simulated PAE, output power and power gain versus input power at 140 MHz.

IV. Conclusion

HiVP configuration has been implemented using lumped components in the hybrid circuit format. The main advantage of this design is its ability to provide high gains at high power levels while achieving a good efficiency. By using four BLF571 LDMOS devices in HiVP configuration, a class-E

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power amplifier has been implemented. More than 30 dB of gain has been achieved with 50 W output power level and PAE of 69% at 150 MHz. This design has been implemented to demonstrate power combining from packaged devices using HiVP. Our aim is to ultimately design a 1.5 KW power amplifier using the same technique for synthetic aperture radar application.

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