

Fabrication and Performance Evaluation of Micromachined Cavity-backed Co-Planar Waveguide to Rectangular Waveguide Transition at Y-band Frequencies

M. Vahidpour *, K. Sarabandi

Radiation Laboratory, EECS Department, University of Michigan, 48105

E-mail: mvahid@umich.edu, saraband@eecs.umich.edu

Introduction

The increasing demand for microwave and millimeter-wave (MMW) monolithic integrated circuits has led to the development and implementation of coplanar waveguides (CPW). CPW lines offer many advantages such as compact planar geometry and ease of integration with shunt and series elements. On the other hand, rectangular waveguides are widely used at higher frequencies as antenna feeds and filters due to their low loss characteristics, and high power handling capabilities. Because of these features, it is common to see submillimeter- and millimeter-wave devices combine waveguide components with CPW lines. For such devices, obviously an appropriate low loss transitions is required. However, as the frequency increases and the dimensions of the line and waveguide shrink, limitations of machining and microfabrication processes are not appropriate for the existing transition designs. The literature concerning microfabricating waveguide structures at W-band and higher frequencies is rather sparse. There have been several attempts to fabricate MMW waveguides with low-cost microfabrication techniques such as lithography [1], [2]. However, in these techniques, the height of the waveguide is limited by the maximum thickness of the spun photoresist, limiting the fabrication to the reduced-height waveguides which suffer from high attenuation. An alternate technique to etch the waveguide is deep reactive ion etching (DRIE) of silicon which provides vertical sidewalls. In [3] and [4], a transition using microfabrication processes with separately fabricated and assembled probe has been reported for both diamond and rectangular waveguide with 20% bandwidth. In this study, we propose a cavity-backed CPW (CBCPW) to rectangular waveguide transition compatible with silicon microfabrication techniques that does not require multiple parts and assemblies. In this approach, the complexity associated with fabrication of suspended probe is eliminated and a compact and wideband transition is achieved using a novel two-pole resonant matching network. The transition is composed of a shorted CPW line over a reduced height short-circuited waveguide segment that is followed by an E-plane step discontinuity to a standard height waveguide. Since the structure is simple with the features aligned with the Cartesian coordinate surfaces, it is highly compatible with microfabrication processes and can be fabricated using multi-stage DRIE of silicon. A scaled model of this transition at Ka-band was fabricated using the standard machining tools, and its performance validated experimentally. In this paper, the same structure is considered for fabrication using silicon micromachining for operation at Y-band (240 GHz) frequencies.

Transition Design and Schematic

The geometry of a back-to-back transition from CBCPW to rectangular waveguide and from rectangular waveguide back to the CBCPW is presented in Fig. 1. The CBCPW [5] is suspended on a membrane layer and is optimized for minimal insertion loss per unit length. The transition consists of CBCPW section, a waveguide section and a transition in which the CPW line is open-circuited and a shorting pin from its center line is terminated to a reduced-height waveguide. The step discontinuity in the E-plane of the waveguide

acts as a capacitive element, it can be used to compensate for the inductive behavior of the shorted pin. That is, a resonant condition can be realized to transfer the power in the transmission line to the waveguide. The length of the waveguide between the pin and the step transition can be used to control the capacitance seen by the inductance. Also, the waveguide height can be used to control the capacitance at the step transition point. Fig. 1 (b) and (c) show the electric field distribution inside the waveguide structure and the S-parameters of a back-to-back transition optimized for this frequency range. It is shown that a reflection coefficient below -20 dB and transmission above -1 dB is achievable for the back-to-back structure over the desired band of 230GHz-245GHz.

For measurement purposes, a transition from the CBCPW line to the conventional CPW is needed. This is because measurement probes cannot be placed over the membrane of the. At the transition from CPW to CBCPW, the vertical wall should not be covered with gold s can, otherwise, the center conductor will be short-circuited (see Fig. 2). The final structure to be fabricated is a transition from CPW to CBCPW and CBCPW to rectangular waveguide.

Microfabrication Processes

A multi-stage approach for etching silicon wafer using deep reactive ion etching (DRIE) method is developed. Unlike wet etchants which etch silicon isotropically along the crystal planes, DRIE is a highly anisotropic etch process used to create deep, steep-sided holes and trenches in wafers, with aspect ratios of 20:1 or more.

When a multi-stage structure is under fabrication, it is required to perform the process in several steps, each time with a different mask. In this process, the wafer is patterned successively with different mask materials which have different etchants and solvents, i.e. they do are not affected by each other's solvents. After patterning the desired mask, the wafer is placed into the STS chamber (DRIE tool) and etched with the first mask to the desired depth and then the first mask is removed. Following this step the wafer is further etched with the second mask to the next level. This process can be continued to achieve trenches and structures with desired heights and depths.

Considering the limitations and selectivity of materials inside the STS chamber and the desired depth levels needed in each etching step, a three step etching is done using silicon oxide, aluminum, and a photoresist masks as shown in Fig. 3 (a). The procedure was performed on a silicon wafer in the following manner: first we deposit a layer of SiO_2 and pattern it with the first mask which has shortest depth and the smallest area. The pattern is shown in yellow color. Then, a metal is used as the second mask. Considering different metals, their etching rate and the amount of roughness they cause due to sputtering during etching, aluminum is found to be a good candidate as a metal mask. A layer of aluminum is evaporated on the patterned SiO_2 layer and is patterned with the second layer mask which produce a lower layer than the previous one. This mask is represented in green color in Fig. 3. Finally a layer of photoresist (for our application PR-SPR 220, PR-S1813 or AZ-9260 can be used) is spun and patterned with the third layer mask which is the bottom layer and has the largest area.

For the DRIE process, this structure is placed inside the chamber and etched to the desired depth (Fig. 3 (b)). Then the first mask (photoresist layer) is dissolved and removed (Fig. 3 (c)). The structure is placed back in the chamber and etched down to the next desired level (Fig. 3 (d)). Then using etchant, the aluminum is removed as well (Fig. 3 (e)) and the wafer is etched with the third mask (Fig. 3 (f)). At the end, the oxide mask is removed. The final three step structure is shown in Fig. 3 (g). Fig. 4 shows the microscopic image of the fabricated three-step structure before and after etching. After the wafer is etched, to make the structure conductive it is placed inside the Enerjet Sputterer for gold deposition. Unlike evaporation in which the sidewalls are not coated

(usually used for lift-off applications), sputtering guarantees sidewall coverage with thickness levels of about 50% flat areas. In order to deposit gold, it is necessary to deposit an adhesion layer first. Chrome is often used as an adhesive layer, but experiments show that Chrome helps silicon to diffuse through gold at high temperature and pressure. This is not desirable as one of the steps in our fabrication is bonding of a top wafer that carries the membrane. In order to perform a very good gold-gold bonding at the next step, the gold layers should be pure. Hence, instead of Chrome, we used Titanium with a thickness of 300 ~ 500 Å which provides a superior diffusion barrier layer between gold and silicon. Then 2 µm of gold is deposited on top to ensure around 1 µm coverage on the sidewalls.

A second wafer is used to cover the top part of the waveguide structure. This wafer contains the patterns of the CPW lines as shown in Fig. 1. Since the lines are suspended on a thin membrane layer as mentioned before, a stacked layer of SiO₂/Si₃N₄/SiO₂ is first deposited on top of the wafer. This layer provides a small amount of stress so that the membrane does not buckle after the wafer is removed. At the next step, this wafer is coated with gold using the Enerjet Evaporator tool with a 500 Å layer of Titanium as a diffusion barrier layer. Then, gold is patterned and etched with the mask of CPW lines. Fig. 5 (a) shows the fabricated top wafer.

At the next step, the top and bottom wafers should be bonded using gold-to-gold thermocompression bonding process. We first need to align the wafers using backside alignment marks and clamp them together. Then they are placed inside the bonding chamber, and a pressure of 4000 torr and temperature of 400°C is applied. Then, the top wafer should be removed to reach the membrane. Fig. 5 (b) shows the top view of the structure after top wafer removal.

References

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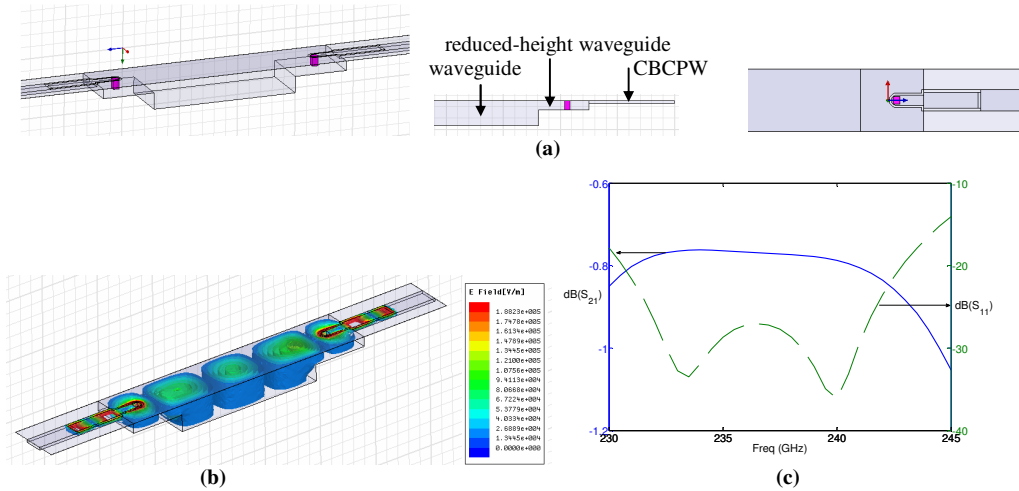


Fig. 1. (a) CBCPW to waveguide transition (b) electric field distribution (c) reflection and transmission coefficients.

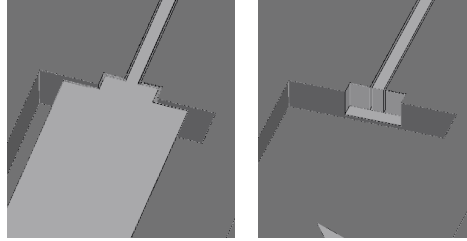


Fig. 2. Conventional CPW to CBCPW transition

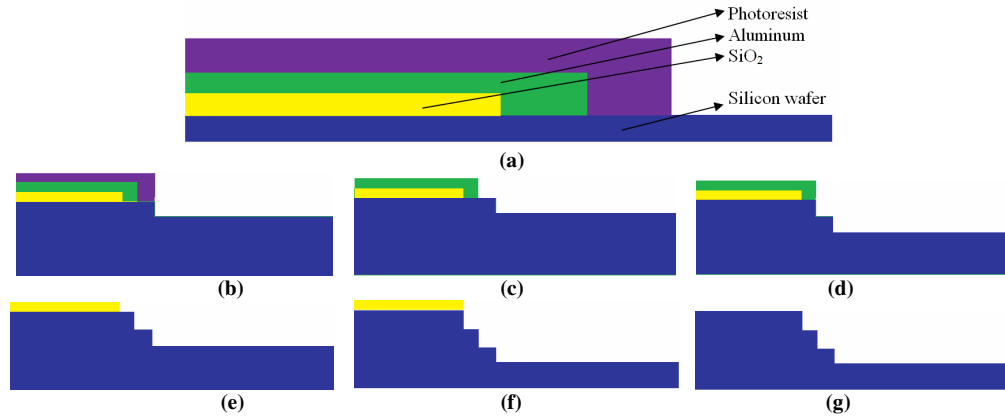


Fig. 3. Microfabrication processes of the multi-stage structure.

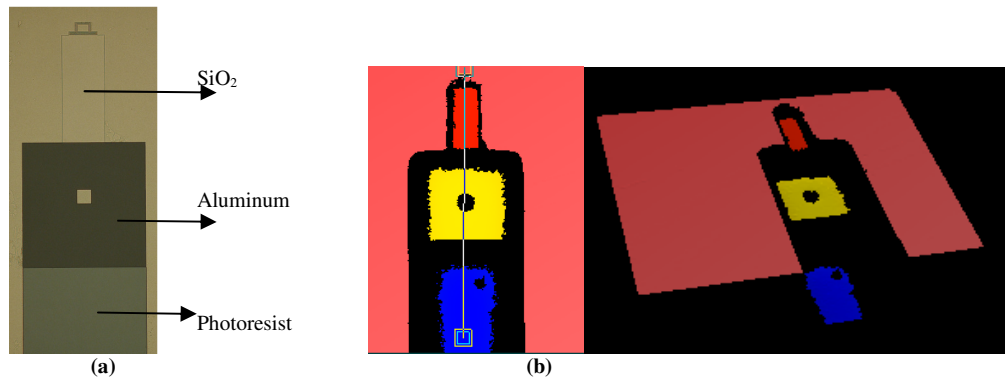


Fig. 4. (a) Three mask layers deposited on a silicon wafer - top view. (b) The structure after etching. The image is taken by a 3D surface profiler tool.

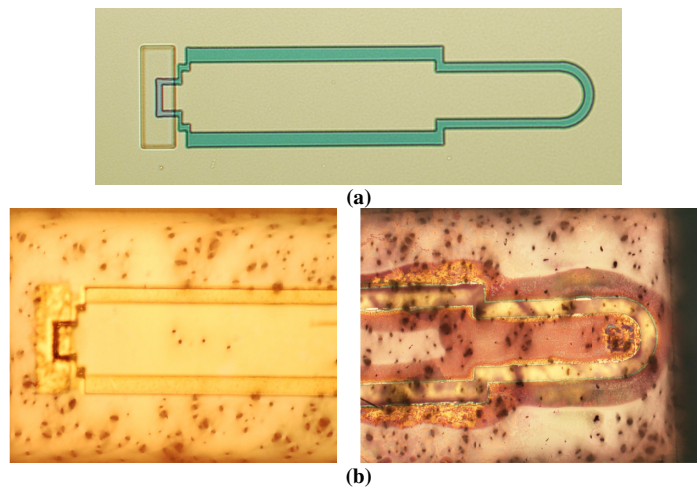


Fig. 5. (a) fabricated top wafer. (b) the structure after bonding and top wafer release.