Micromachined Low-mass RF Front-end for Beam Steering Radar

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ABSTRACT

Sensors for autonomous small robotic platforms must be low mass, compact size and low power due to the limited space. For such applications, as the dimensions of the structures shrink, standard machining methods are not suitable because of low fabrication tolerances and high cost in assembly. Commonly, the structures show a high degree of fabrication complexity due to error in alignment, air gaps between conductive parts, poor metal contact, inaccuracy in patterning because of non-contact lithography, complex assemblies of various parts, and high number of steps needed for construction. However, micromachining offers high fabrication precision, provides easy fabrication and integration with active devices and hence is suitable for manufacturing high MMW and submillimeter-wave frequency structures. A radar design compatible with micromachining process is developed to fabricate a Y-band high resolution radar structure with a slot-fed patch array antenna. A multi-step silicon DRIE process is developed for the fabrication of the waveguide structure while the slots are suspended on a thin oxide/nitride/oxide membrane to form the top cover of the waveguide trenches and the patch elements are suspended on a thin Parylene membrane. Gold thermocompression bonding and Parylene bonding are used to assemble different parts of the antenna. These processes result in a compact (4.5 cm $\times$ 3.5 cm $\times$ 1.5 mm) and light-weight (5 g) radar.

I. INTRODUCTION

The frequency bands of commercial MMW radars are mostly at 77 and 94 GHz for automotive and imaging radars, respectively. With advances in MMIC technology, the applications in these bands have increased and hence the available bandwidth has decreased. In addition, recent demands for very high resolution radars highlighted the need for developing new methods for low-cost and low profile MMW radars at higher MMW frequencies. This requires advances in modern circuitry, digital signal processing techniques and FMCW waveform. There have been several attempts to realize high resolution compact radars at 140 and 220 GHz especially for short range applications with external aperture-type antennas such as horn antennas or integrated antennas such as planar antennas. However, in most of these systems, antenna integration is still a challenge mainly because the antennas are bulky and provide simple functionality; while the size, weight and cost of these radars have to decrease in order to be compatible for small moving platforms and mass productions. For this purpose, low-loss, compact, and fully integrated antennas with more sophisticated performance are required.

In this paper, a two-dimensional micromachined meander-line frequency scanning array based on WR-3 rectangular waveguide is presented for Y-band applications. The structure is capable of achieving $\pm 25^0$ scanning around the broadside angle. A narrow 2^0 beamwidth is achieved in the azimuth direction using linear array of slots that are cut on the broad wall of the waveguide. Employing hybrid-coupled patch arrays, a fixed beam can be realized to present a fairly narrow beamwidth in the elevation direction as well. The waveguide is fed through a membrane-supported cavity-backed CPW with the output of a frequency multiplier providing 230 ~ 245 GHz FMCW signal. It employs waveguide and planar technologies for passive and active components respectively. The passive components include slot-fed meanderline waveguide patch array, CPW-waveguide transition and waveguide filters. A novel microfabrication method using three separate silicon wafers is developed to fabricate the radar.
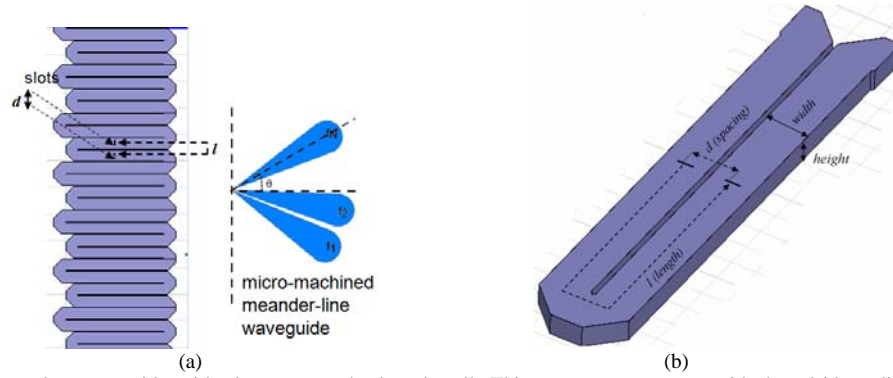
Fig. 1. (a) Rectangular waveguide with slots cut on the broad wall. This structure cannot provide broadside radiation without generating grating lobes. The scanning range is also limited. (b) Waveguide-based helical slot antenna. (c) Planer meander-line waveguide slot antenna (d) unit cell of the proposed structure.

II. RADAR DESIGN

The structure under investigation is shown in Fig. 1 (a) in which slots are cut along the walls of a meanderline waveguide in order to achieve broadside radiation and a satisfactory amount of phase shift between elements without the need for a large bandwidth. In this design, the waveguide is bent around the H-plane to have the radiating elements cut on the broad wall of the waveguide so that microfabrication techniques are able to manage etching the height of the waveguide which is more endurable than etching the thick width of the waveguide. In this structure, $\psi = kd\sin(\theta) + \beta l$ where d is the spacing between elements which is the sum of the waveguide width and the separating wall, while l is the length between them in each turn as shown in the unit cell of the structure in Fig. 1 (b). Hence, while it is feasible to realize broadside radiation at any desired frequency with $\beta l = 2n\pi$ since l is flexible; the maximum scanning angle can also be calculated as

$$\theta_1 = \sin^{-1}\left(\frac{l\lambda_1}{d}(\frac{1}{\lambda_{g0}} - \frac{1}{\lambda_{g1}}) \right) \qquad (1)$$

To have the broadside radiation at the center frequency, l is chosen to be a modulus of λ_{g0} in order to generate $2n\pi$ phase shift between the elements at the center frequency. Table I shows the range of scanning angle assuming 15 GHz available bandwidth (230 ~ 245 GHz) around the broadside radiation at 237.5 GHz for different values of wall thicknesses and length between elements. To achieve a very narrow beamwidth (i.e. $\alpha = 2^0$), the length of the antenna must be extended by using a number of these unit cells. The length is calculated from

$$\alpha = \frac{\lambda}{L} \Rightarrow L = \frac{\lambda}{\alpha} \qquad (2)$$

where, L is the aperture length. At 230 GHz, $L = 37.4$ mm to achieve 2^0 beam width, which give around 36 turns for $t = 1114$ μm.

Since the overall waveguide length is quite large (~ 36 l = 36cm), and a large number of slots are involved, sources of loss and reflection from the finite conductivity of metals, waveguide turns, and slots must be managed very carefully.

Table I. The scanning angle of the antenna for different wall thicknesses and lengths between elements.

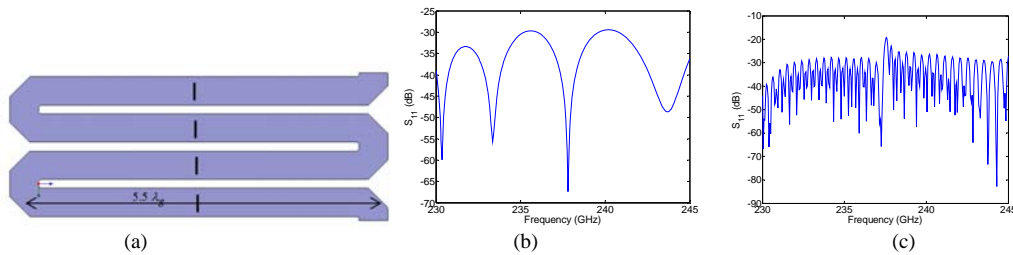| Thickness of the separating wall $d = a + t$	Length between the elements	Range of the scanning angle
$t = 50$ μm	$l = 4 \lambda_{g0}$	$23.3^0 \sim -21^0$
$t = 150$μm	$l = 5 \lambda_{g0}$	$26.4 \sim -23.7^0$
$t = 250$μm	$l = 5 \lambda_{g0}$	$24^0 \sim -21.8^0$
$t = 50$ μm	$l = 4.5 \lambda_{g0}$	$26.4^0 \sim -23.7^0$
$t = 250$μm	$l = 5.5 \lambda_{g0}$	$26.5^0 \sim 23.8^0$

Fig. 2. (a) The unit cell of the meander-line structure with 250 µm separating walls optimized for minimum reflection at the beginning and end of the band. (b) Reflection coefficient for the unit cell. (c) Reflection coefficient for nine unit cells

A. Reflection

There are two sources of reflection in the meander-line structure: from the bends and from the slots. To minimize the reflection from the bends, the profile of the bends should be designed for a minimum reflection. This can be performed by optimizing the shape of the bends using Ansoft HFSS. Simulations results show that a diagonal cut around the edges provides a better transmission compared to a curved turn. However, even though the reflection from bends is minimized, a number of successive small reflections from all bends make a considerable amount. To minimize the total reflection, the waveguide length is designed to generate constructive interference for the center frequency, since the reflection of the bend is already minimized by optimizing the diagonal cut. In this case, the reflection in the beginning and the end of the band is minimized by changing the thickness of separating walls to make the destructive interference. The reflection coefficient of the structure is shown in Fig. 2 (b) and (c) for one and nine unit cells. The maximum reflection is below -18 dB as opposed to -2 dB reflection for the former structure, while the reflection at the center frequency is maintained around -60 dB. This structure has thicker separating walls which makes it stiffer and suitable for microfabrication.

To minimize the reflection of the slots, having cut one slot in each turn, the two-way distance between two successive slots is an integer multiple of λ_g ($2 \times 5.5 = 11 \lambda_g$ in this design). Therefore, their successive reflections add up coherently and causes scan blindness at the center frequency. To mitigate this problem we need a reflection canceling pair for each slot positioned at $\lambda_g / 4$.

B. Conductor Loss

In a rectangular waveguide, the conductor loss is calculated from

$$\alpha = \frac{R_m (2bk_c^2 + ak_0^2)}{ab\beta_{TE_{10}} k_0 Z_0} \tag{3}$$

where $R_m = \sqrt{\dfrac{\omega\mu_0}{2\sigma}}$, σ is the electrical conductivity, k_c the cut-off frequency of the waveguide, k_0 wavenumber, Z_0 free space characteristic impedance, a and b are width and height of the waveguide. In 230~245 GHz band, $\alpha \approx 18$ dB/m for gold and 16 dB/m for copper and the total loss for the meander-line structure is around 6.6 dB for gold and 5.9 dB for copper which mean around 20% of the power reaches the end of the waveguide. The amount of radiated power from slots should be managed accordingly in order to have a uniform power distribution for each element.

C. Slot Positioning and Shape

Transverse slots are not commonly used in array applications for broadside radiation mainly because the spacing is twice as much the longitudinal slots which results in grating lobes. However, they are successfully used in traveling-wave arrays for off-broadside radiation and are suitable for the application of this work since the spacing is already smaller than half a wavelength and the length required to generate the desired phase shift is provided by the length of the meander-line structure. In addition, the main role of the slots is to feed the patch array and since the patch should provide narrow beam in the elevation direction, it should be positioned along the waveguide. For the array positioned along the waveguide, transverse slots are the only options for excitation. At the resonant frequency, the amount of radiated power and thus the radiation resistance of a slot is maximized as shown in Fig. 3 (a) that represents a resonant frequency around 282 GHz. However, since in a large array it is mostly desirable to distribute the power evenly among the elements, small amount of power is apportioned to each slot and thus the slots should be non-resonant. Therefore, the dimensions of the slots are chosen to be much smaller than $\lambda_0/2$ to make them non-resonant. This causes non-zero reactive part for radiation power. This is compensated later by using patches on top of the slots which make them resonant although the length is not $\lambda_0/2$. By changing the dimensions of the slots, we can control the amount of radiated power off of each slot. Fig. 3 (b) shows the total power associated with a non-resonant slot (radiated plus stored) for slots with around $\lambda_0/4$ length at two different widths. Since the amount of propagating energy is decreased along the waveguide as it is partly radiated and stored around each slot, and lost due to the finite conductivity of metal, the dimensions of the slots should be increased gradually so that the radiated power remains constant throughout the length of the waveguide even though the input power is decreased. To design the slot dimensions, first we assume that the radiated power from the four adjacent slots in each turn is constant. Therefore, considering the conductive loss, in each turn

$$P_2 = P_1 - 4\alpha_s P_1 - \alpha_c P_1 \qquad (4)$$

where, P_1 and P_2 are the input and output powers in the waveguide, α_c is the percentage of the conductive loss and α_s the percentage of the radiated power off of each slot. For the next turn, the amount of the input power is decreased to P_2 hence α_s for each slot should be increased so that the total power $\alpha_s P$ remains constant. Again the input power in the third turn decreases and the dimension of the slots should be increased. According to this design, we start from slots with 300 μm × 5 μm dimensions for the first turn and end with those with 300 μm × 60 μm for the last one.
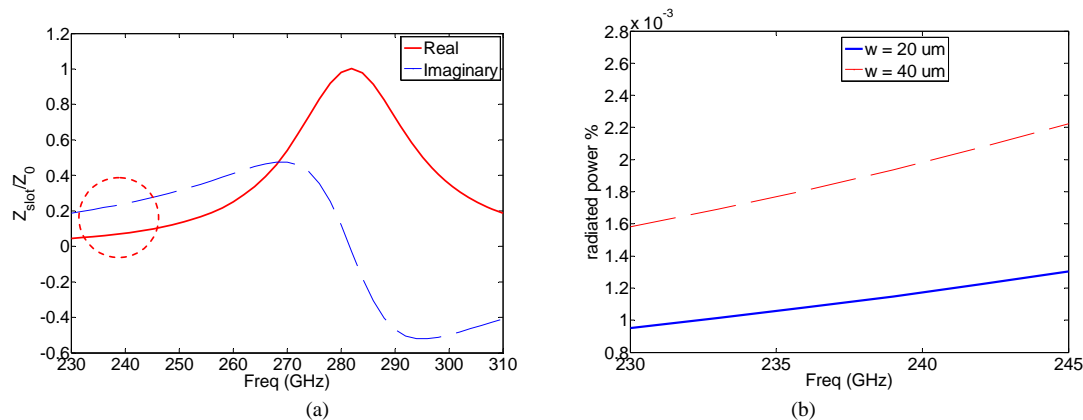
Fig. 3. (a) Normalized slot impedance versus frequency. A resonance happened at 282 GHz. (b) The total power associated with a non-resonant slot for two different widths.

D. Hybrid-Coupled Patch Array

The one-dimensional array of slots generates a very wide beam in the elevation direction. For many applications ranging from collision avoidance to indoor mapping, this wide beamwidth is not desirable due to the possibility of the interference caused by other targets. In order to confine the beam, we need to provide a long aperture in that direction as well. This can be performed by designing patch arrays which are fed by these slots.

A hybrid-coupled patch array proposed to provide a narrow beam in the elevation direction. In these arrays, the patches are positioned on top of the slots separated by a dielectric substrate. The center patch is fed by the slot on the bottom layer of the substrate, while the other patches are series-fed through the center one. The feeding is a combination of both planar and non-planar feeding methods. The main advantage of this coupling method is the ability to control the illumination function separately in both array directions in order to produce a specified radiation pattern so that while the pattern is scanning in the azimuth direction, it is fixed in the elevation direction.

However, there are some problems associated with patch antennas at high frequencies, such as very thin substrates are required in order to suppress the propagation of the surface waves. For example, at 230 GHz, 50 μm glass or 20 μm silicon substrates are only around one tenth of the guiding wavelength and it is almost impossible to handle these very thin substrates. Yet at the same time, they are thicker than what can be spun or deposited specifically for most commonly used low-loss materials (such as spin-on glass which can be spun up to 5 μm). Hence, using a dielectric substrate for the patch array is not desired. Instead, air substrate can be used and the patch array is suspended on a thin layer of dielectric material. With air substrate, no surface waves are excited, bandwidth is improved and the efficiency is highly enhanced. To provide efficient slot-patch coupling, the thickness of the air substrate should be kept below 100 μm. For thicker substrates, the coupling is weakened as shown in Fig. 4 (a) and (b). As mentioned before, hollow structures are fabricated using silicon bulk micromachining. Since patches and slots are fabricated on either side of the substrate, custom-made, non-standard ultra-thin wafers have to be used with precise thickness as the substrate. These substrates are expensive and hard to handle. To make the structure more robust for fabrication, the feasibility of using thick standard substrate is investigated. As shown in Fig. 4 (c) incorporating dielectric walls confine the field under the patch. The idea stems from the fact that the vertical field component of the slot adjacent to the dielectric wall with a higher dielectric constant is enhanced; since the tangential component of the electric field remains the same while the normal component is decreased by the ratio of dielectric constant of the two media. Therefore, the field is bent toward the boundary. Although a single patch may now be excited on thick substrate, the rest of the array can take advantage of a thin substrate by suggesting the structure shown in Fig. 5 (a), in which the center patch is fed through the slot with the thick air substrate and dielectric block, while the rest of the patches are series-fed with the original thin substrate. This structure can be fabricated on a thick standard wafer which is more robust. The optimized simulation results show low side-lobe level and acceptable directivity over the band shown in Fig. 5 (b) and (c).
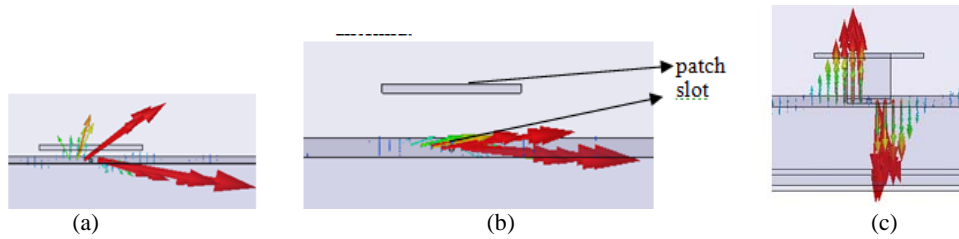
Fig. 4. Field distribution for air substrate at 230 GHz (a) 80 um substrate (b) 250 um substrate (c) 250 um substrate with silicon walls
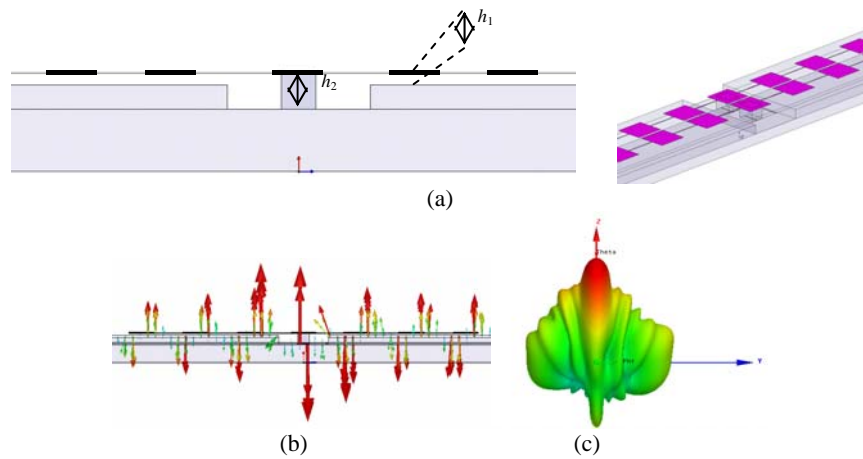

Fig. 5. (a) The proposed hybrid-coupled patch array with silicon block. (b) The electric field distribution (c) the radiation pattern at the center frequency 237.5 GHz and.

E. The Final Design

The final antenna structure and the radiation pattern in the azimuth direction are shown in Fig. 6 (a) and (b). It is noticeable that the main beam is steering from -24^0 to $+26^0$ by changing the frequency from 230 GHz to 245 GHz. The scan angle for different frequencies is listed in Table I. The structure is fed through a transition to membrane supported CBCPW line.
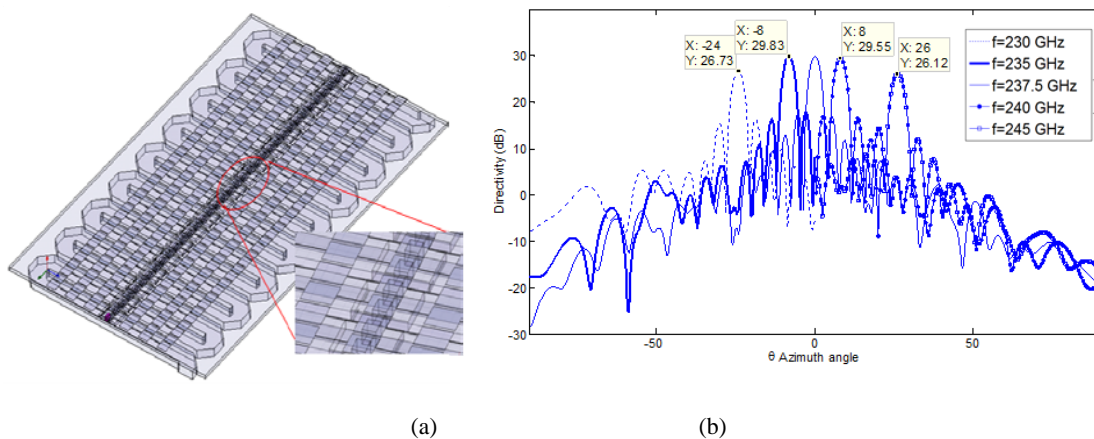

Fig. 6 (a) final antenna structure and (b) the radiation pattern

Table I. Different scan angles versus frequency to verify frequency scanning.

Frequency	Scan angle	Directivity
230 GHz	-24 deg	26.73 dB
235 GHz	-8 deg	29.83
237.5 GHz	0 deg	29.87
240 GHz	8 deg	29.55
245 GHz	26 deg	26.12

III. MICROFABRICATION PROCESS

The radar structure includes WR-3 waveguide trenches, membrane-supported CPW, slot array and patch arrays. The complete structure does not incorporate any dielectric material and is fabricated on three separate silicon wafers to form the waveguide trenches, slot arrays and patch arrays as shown in Figure.1. The meander-line waveguide is etched on a wafer, the slots are etched on another wafer and bonded to the first wafer, and finally the patch arrays are patterned on a third wafer and then bonded to the structure.
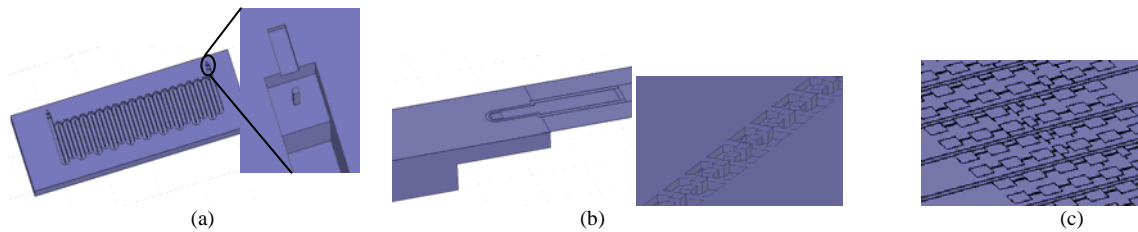

| (a) | (b) | (c) |

Figure.1. The radar structure fabrication steps. (a) First wafer includes waveguide trench and multi-step structure of the waveguide transition (b) Second wafer includes slots and CPW line patterns with the patch substrate on the other side (c) Third wafer includes the patch arrays. The wafers are connected using wafer bonding processes.

A. First Wafer - Meander-line Structure

To create a multi-step structure required for waveguide transitions on a silicon wafer, the wafer is patterned successively with different mask materials. It is etched with the last mask to the desired depth. Then the mask is removed and etching is continued with the next mask to the desired depth for the next step. After the wafer is etched, a layer of silicon dioxide is deposited as a diffusion barrier before metalizing the surface with gold. This layer is needed for next step of wafer-to-wafer gold bonding to stop diffusion of silicon through the gold layer at high temperature and pressure and to prevent eutectic bonding.. For gold deposition, a sputtering tool with sidewall coverage capability is used which guarantees coverage of around 50% of the value on the exposed surfaces. In order to deposit gold, it is necessary to deposit an adhesion layer first. Experiments showed that a chrome layer alone does not prevent silicon diffusion through gold at high temperature and pressure. Either titanium or a combination of chrome and titanium with thicknesses of 300 ~ 500 A^{o} provides a superior diffusion barrier layer between gold and silicon. The minimum gold thickness of 1.2 μm is needed in order to ensure at least 0.5 μm of gold is deposited on the sidewalls. Figure.2 shows the microscopic image of the fabricated three-step meander-line waveguide, back-to-back transition and the waveguide filter.
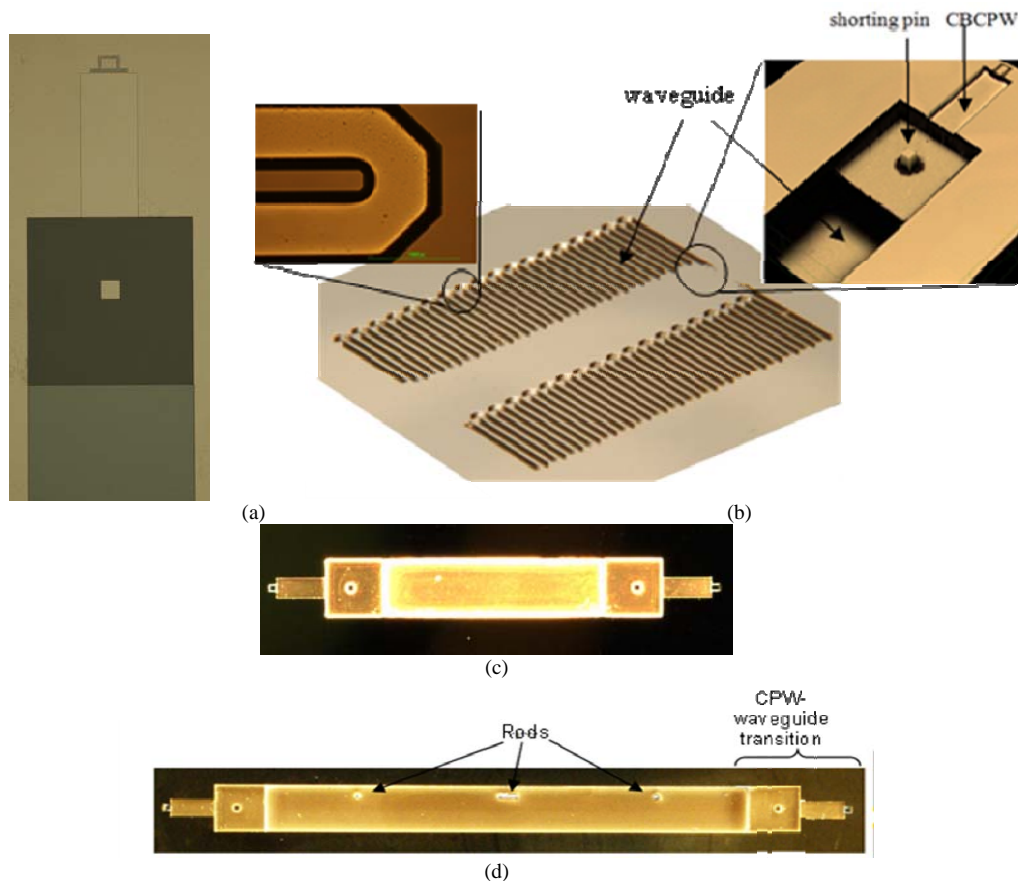
Figure.2. (a) Three-step patterning the waveguide. (b) Meander-line waveguide. (c) back-to-back CBCPW to waveguide transition. (d) waveguide filter with the transition

B. Second Wafer –Slots / Patch Array Substrate

A second wafer is used to cover the top part of the meander-line structure, which includes the CPW lines and slots. This wafer also serves as the substrate of the patch arrays. Two variations of the structure were fabricated at this stage. A simpler process was developed to fabricate the transition, filters and slot-waveguide antenna. A second process is proposed to fabricate the hybrid-coupled patch array which needs a third wafer. Since the CBCPWs are suspended on a thin membrane layer, a stacked layer of LPCVD $SiO_2/Si_3N_4/SiO_2$ (ONO) is first deposited on top of the second wafer. This layer provides a small amount of tensile stress so that the membrane does not buckle after the wafer release. The wafer is then gold-coated with an adhesion layer, and then patterned and etched to form the CPW lines as well as the slots. Then it is flipped over and the backside is etched to form openings on top of the CBCPW and the slots. The structure is suspended on a membrane around the open areas of the wafer and should be carefully handled. Figure.3 illustrates the fabrication process of this wafer and Figure.4 shows the fabricated CPW lines and slots on the gold side of the wafer. At this stage, the first and second wafers should be bonded. Since the wafers are gold covered, we have to perform gold-to-gold thermocompression bonding. This bonding technique provides a hermetic of the surfaces and guarantees the continuity of the current flow. One concern however, is diffusion of silicon through gold, introducing impurities and failure in bonding. To overcome this problem, as mentioned before, a SiO_2 diffusion barrier layer before gold deposition is necessary [1]. The stacked membrane layer already serves as the diffusion barrier on the second wafer. The wafer alignment can be performed using backside processing of alignment marks or top side alignment through the transparent membrane. After aligning and clamping the wafers, they are placed inside the bonding chamber and a pressure of 3000 ~ 4000 torr and temperature of 375^0 ~ 400^0c is applied for 40 minutes [2], [3]. Mechanical robustness of gold bonding has been verified by dicing and examining the bonded wafers at multiple locations. Visual inspections and mechanical tests to separate the segments of bonded wafers all

indicated very high quality gold-to-gold bonding. The process is shown in Figure.5 and the fabricated slot-waveguide array, CBCPW to waveguide transition and CPW and CBCPW lines for calibration are presented in Figure.6.

To fabricate the patch array version of the antenna structure, after CPW/slot patterning on the second wafer, the backside is etched with a different pattern. While silicon is still completely removed from the areas around the CBCPW membrane, the pattern of the patch substrate is etched around the slots with the pattern shown in Figure.7 (a). We perform a multi-step etching for the substrate with a similar process mentioned for the first wafer with the membrane as the etch stop of the process. Then the substrate is gold-coated as shown in Figure.7 (b). Due to the RIE lag effect, the etch depth is dependent on the etched area, i. e., it is deeper for larger areas. Figure.7 (c) shows a more realistic figure of what is realized after etching. This issue is addressed by simulating such a structure. The results show a similar performance for etches deeper than 60% which indicates the steps do not cause a noteworthy change in the antenna pattern and the reflection loss.

The wafer is then bonded to the first wafer as shown in Figure.8 with the same gold-gold bonding process. Figure.9 shows the fabricated patch array substrate.
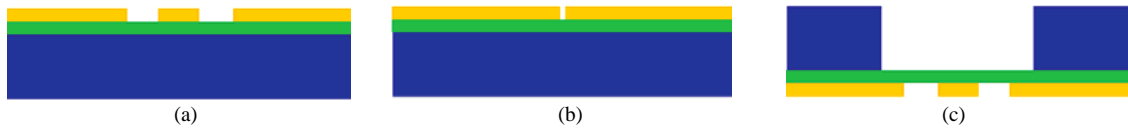

| (a) | (b) | (c) |

Figure.3. Second wafer fabrication process. A stacked layer of LPCVD SiO_2/Si_3N_4/SiO_2 (ONO) as a membrane followed by gold is deposited. Then gold is patterned with the mask of (a) CPW and CBCPW lines. (b) the slots. (c) The wafer is flipped over and the backside is etched from the top of the areas around CBCPW and slots.

| (a) | (b) |

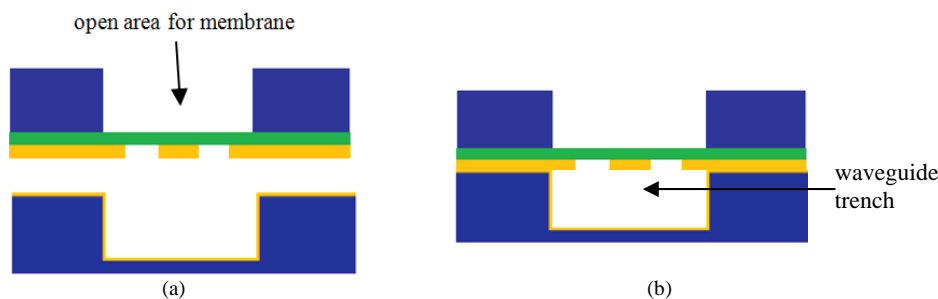Figure.4. Fabricated second wafer. (a) top side- CPW/CBCPW lines (b) top side - slots

open area for membrane

waveguide trench

| (a) | (b) |

Figure.5. First and second wafers. (a) before gold-gold thermocompression bonding (b) after bonding
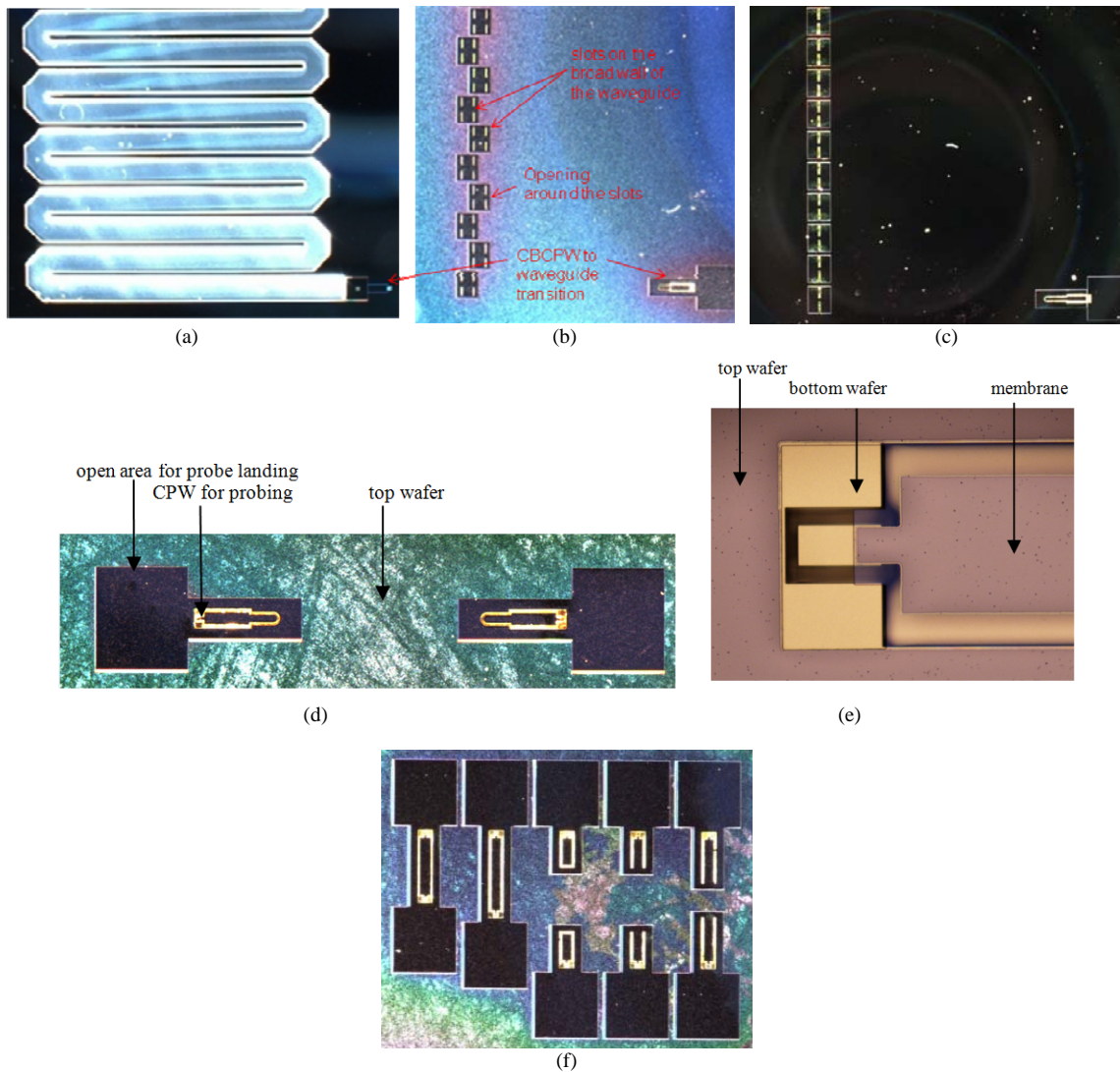
(a)

(b)

(c)

(d)

(e)

(f)

Figure.6. (a) First wafer before bonding. (b) the meander-line slot antenna after bonding, (c) the low-loss design (d) the CBCPW/waveguide transition, (e) the CPW/CBCPW transition, (f) calibration standards, from left to right: thru, line, open, short, offset short.
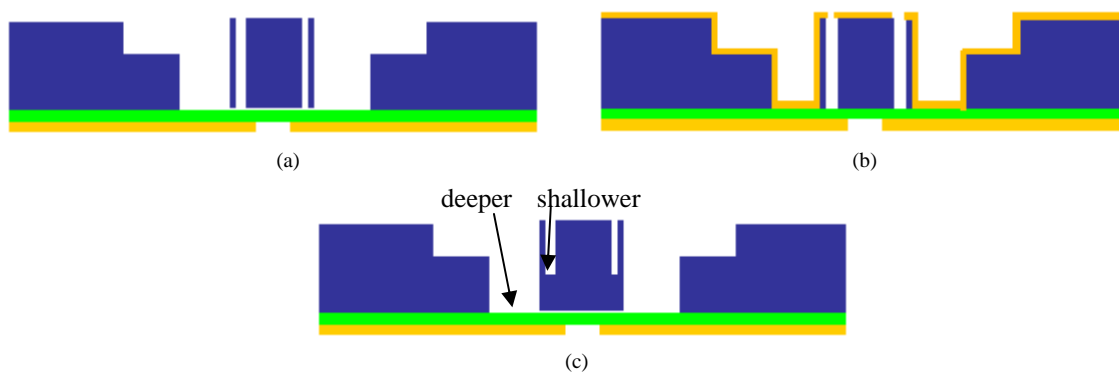

(a)

(b)

deeper   shallower

(c)

Figure.7. (a) multi-step etching for the patch array substrate. Thin shadow walls are also formed to protect the sidewalls of the silicon block from gold-deposition. (b) gold-coating the substrate. (c) the realistic version of the structure.
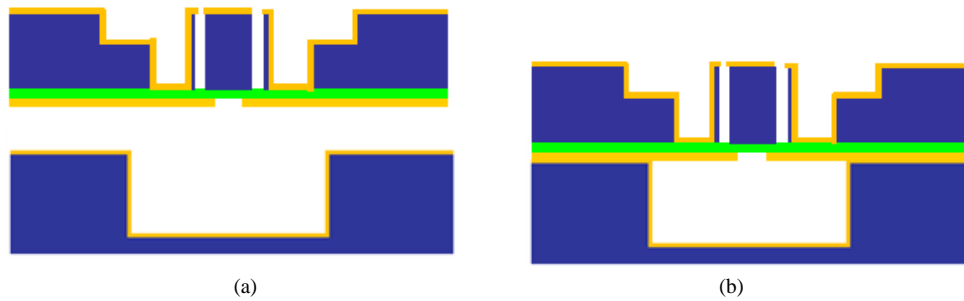
(a)   (b)

Figure.8. First and second wafers. (a) before gold-gold thermocompression bonding (b) after bonding
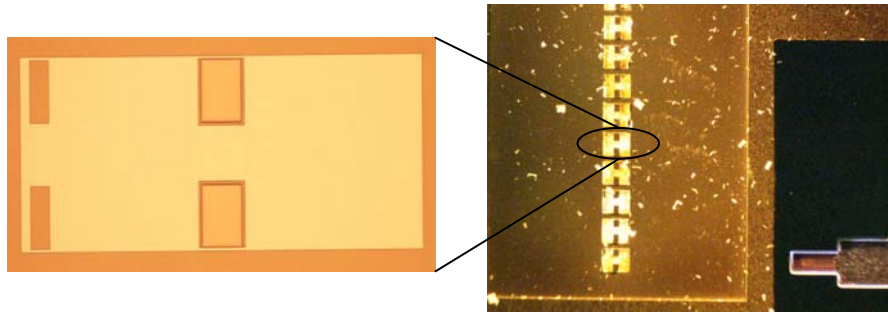

Figure.9. Fabricated patch array substrate

C. Third Wafer –Patch Array

The patch array structure consists of $36 \times 2 = 72$ (two in each turn) seven-element patch sub-arrays (total of 504 patches). The array has to be suspended over a membrane on top of the air substrate. The fabrication process is illustrated in Figure.10. First, to make a membrane layer with a low adhesion with the wafer, a layer of a photoresist (as a release layer) is spun on the unpolished side of a silicon wafer and baked. Using the unpolished side of the wafer helps decrease the adhesion of the Parylene membrane to silicon after removing the release layer. Then, a layer of Parylene with 5 ~ 15 um thickness and then gold is deposited and patterned to form the patch arrays. At the last step, we make some cuts on the Parylene around the circumference of the wafer to provide access to the bottom photoresist layer. The wafer is soaked in acetone and then IPA (isopropyl alcohol) solutions for several days to dissolve the photoresist completely as shown in Figure.10 (b). The fabricated third wafer is shown in Figure.11.

Since Parylene, like other polymers, very efficiently bonds to itself, the gold-bonded pair should also be covered with Parylene first as shown in Figure.12 (a). This layer could be very thin (< 5 µm) in order not to affect the patch array loss. Parylene bonding is performed under vacuum in order to avoid Parylene interaction with oxygen and nitrogen at 150+ ^{0}C and 800 N force over a 4 inch wafer for 30~40 minutes. For this very structure, bonding pressure should be much higher (5000 ~ 7000 N) than usual since the gold-bonded pair is bowed by a small amount and we have to compensate for it to make sure the Parylene layers are in contact everywhere on the wafer.

The patch array membrane is transferred after bonding. A razor blade can used to cut the Parylene from the circumference of the third wafer so that the wafer is debonded and released as shown in Figure.12 (d). Since the Parylene from the patch wafer is connected to the bottom Parylene wafer, this method is called the Parylene transfer method [3]. Figure.11 shows the fabricated Parylene membrane.

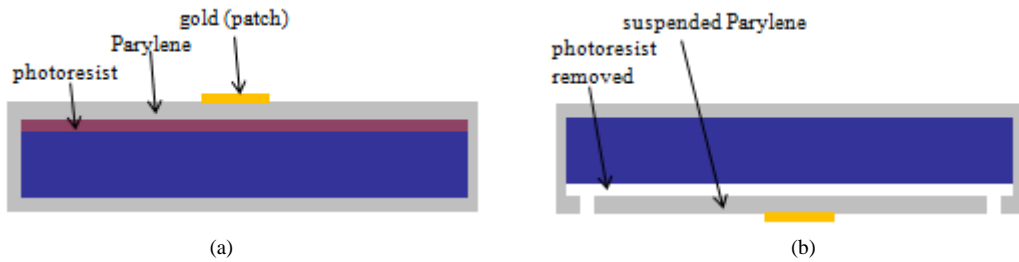(a)   (b)

Figure.10. Third wafer fabrication process. (a) photoresist, Parylene and patterned gold are deposited on a silicon wafer. (b) photoresist is dissolved by soaking the wafer in acetone and IPA.
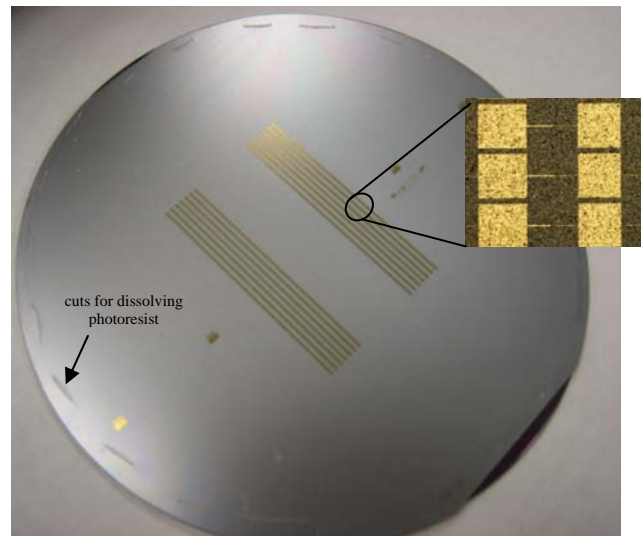

Figure.11. Fabricated third wafer after dissolving the photoresist release layer.

(a)   (b)

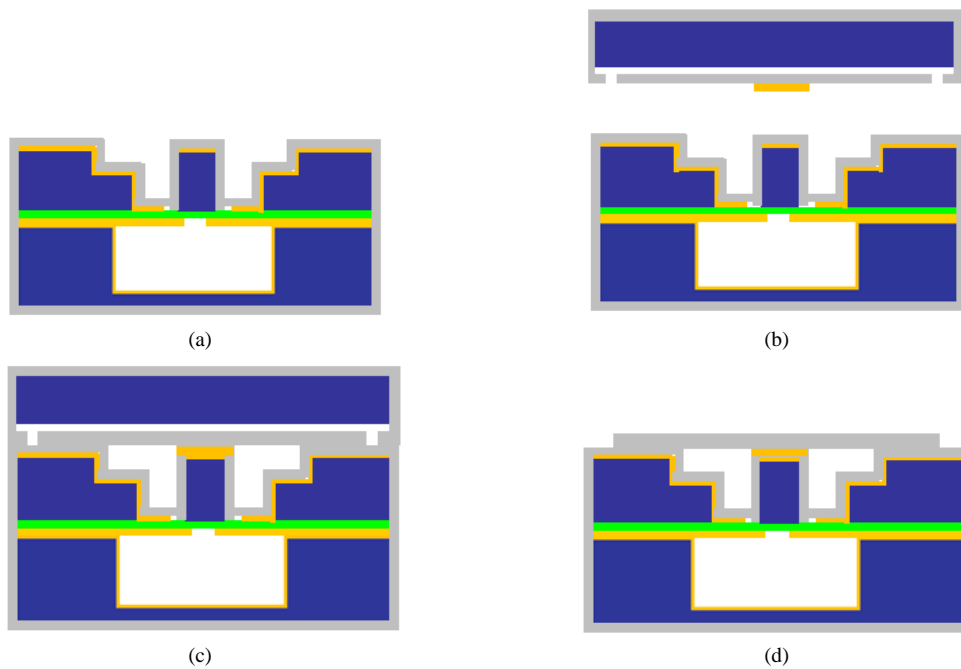(c)   (d)

Figure.12. Last step of the fabrication process. (a) The gold-bonded pair is Parylene-coated. (b) The wafers are aligned and (c) bonded. (d) The third wafer is de-bonded with a razor blade through the edges.
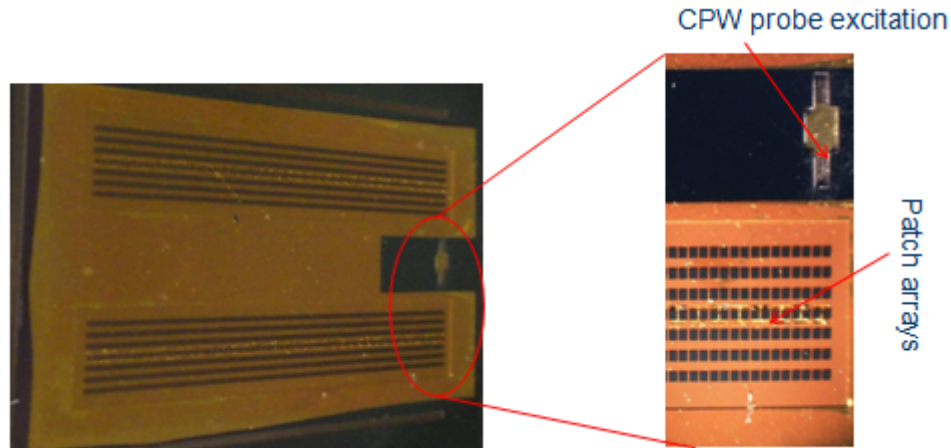
Figure.13. Final fabricated structure.

IV. CONCLUSION

A novel radar design compatible with micromachining techniques is proposed for Y-band applications. This structure is capable of achieving $\pm\,25^{0}$ scanning around the broadside angle. A narrow 2^{0} beamwidth is achieved in the azimuth direction using linear array of slots cut on the broad wall of the waveguide. Employing hybrid-coupled patch arrays, a fixed beam can be realized to present a fairly narrow beamwidth in the elevation direction as well. The waveguide is fed through a membrane-supported cavity-backed CPW which is the output of a frequency multiplier providing 230 ~ 245 GHz FMCW signal.

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