Comments and Corrections

Correction to "A Power-Efficient 32 bit ARM Processor Using Timing-Error Detection and Correction for Transient-Error Tolerance and Adaptation to PVT Variation"

David Bull, Shidhartha Das, Karthik Shivashankar, Ganesh S. Dasika, Krisztian Flautner, and David Blaauw

In the above paper [1], Fig. 12 was printed incorrectly. The correct figure is shown below. We sincerely regret the error.

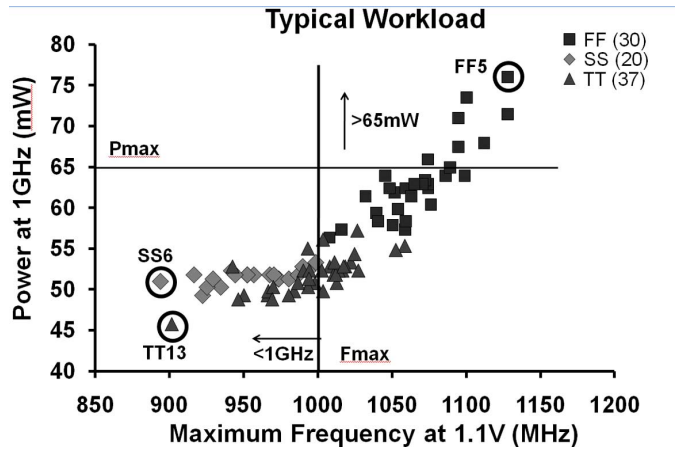

Fig. 12. Power at 1 GHz for typical workload versus silicon-grade measured by highest frequency for correct operation without Razor at 1.1 V constant VDD. Measurements obtained on 87 die from split lots. Yield window is shown for frequency target (Fmax) of 1 GHz and power target (Pmax) of 65 mW.

Manuscript received January 28, 2011. Date of current version February 24, 2011.

D. Bull, S. Das, K. Shivashankar, and K. Flautner are with ARM Inc., Cambridge CB1 9NJ, U.K. (e-mail: dbull@arm.com, sdas@arm.com, karthik.shivashankar@arm.com, krisztian.flautner@arm.com).

G. S. Dasika and D. Blaauw are with the University of Michigan, Ann Arbor, MI 48109 USA (e-mail: gdasika@eecs.umich.edu, blaauw@umich.edu).

Digital Object Identifier 10.1109/JSSC.2011.2111230

References

[1] D. Bull, S. Das, K. Shivashankar, G. S. Dasika, K. Flautner, and D. Blaauw, "A power-efficient 32 bit ARM processor using timing-error detection and correction for transient-error tolerance and adaptation to PVT variation," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 18–31, Jan. 2011.