Sleep Mode Analysis and Optimization With Minimal-Sized Power Gating Switch for Ultra-Low $V_{\rm dd}$ Operation

Mingoo Seok, *Student Member, IEEE*, Scott Hanson, David Blaauw, *Fellow, IEEE*, and Dennis Sylvester, *Fellow, IEEE*

***Abstract*—This paper investigates the optimization of sleep mode energy consumption for ultra-low $V_{\rm dd}$ CMOS circuits, which is motivated by our findings that minimization of sleep mode energy holds great potential for reducing total energy consumption. We propose a unique approach of using a power gating switch (PGS) in ultra-low $V_{\rm dd}$ regimes. Unlike the conventional manner of using PGSs, our optimization suggests using minimal-sized PGSs with a slightly higher $V_{\rm dd}$ to compensate for voltage drop across the PGS. In SPICE simulations, this reduces total energy consumption by $\sim 125\times$ compared to conventional approaches. The effectiveness of the proposed optimization is also confirmed by measurements taken from an ultra-low power microprocessor. Additionally, the feasibility of using minimal PGSs in ultra-low $V_{\rm dd}$ regimes is investigated using SPICE simulations and silicon measurements.**

***Index Terms*—MTCMOS, power gating switch, sleeps mode, standby mode, subthreshold operation, ultra-low power.**

I. Impact of Sleep Energy on Total Energy Consumption

VOLTAGE scaling is well known as an effective method to reduce energy-per-operation due to the quadratic relationship between switch energy ($E_{\rm switch}$) and supply voltage. Therefore, dynamic voltage scaling (DVS) has been used in microprocessors to scale down the supply voltage to the point where a task is completed just before the deadline, thereby saving a significant amount of energy [1], [2].

However voltage scaling has limitations in providing energy savings [3]. Metal oxide semiconductor field effect transistors (MOSFET) become exponentially slow once the supply voltage scales below the threshold voltage ($V_{\rm th}$) of devices due to the small subthreshold current, as captured by the well-known subthreshold current (1). This performance degradation causes a rapid increase of leakage energy ($E_{\rm leak}$), which eventually offsets the savings of $E_{\rm switch}$. Therefore, the total energy consumption starts to increase once the supply voltage scales down below a certain point, which we refer to as $V_{\rm min}$. The optimal energy consumption, which occurs at $V_{\rm min}$, is defined as $E_{\rm min}$. This relationship is illustrated in Fig. 1 and analytically modeled in (2) [3]

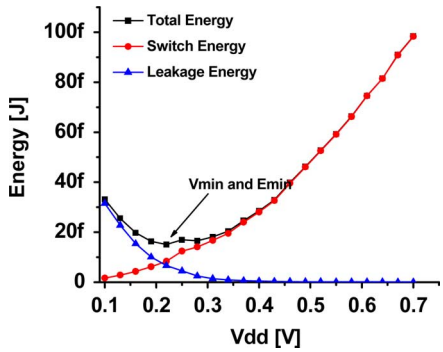

Fig. 1. $V_{\rm min}/E_{\rm min}$ curve with no consideration on sleep energy.

$$\begin{aligned} I_{\rm sub} &= \mu \cdot {\rm Cox} \cdot W/L \cdot (m-1) \cdot V_T^2 \\ &\quad \cdot \exp\left(V_{\rm gs} - V_{\rm th}/mV_T\right) \\ &\quad \cdot \left(1 - \exp(-V_{\rm ds}/V_T\right) \end{aligned} \tag{1}$$

$$\begin{aligned} E &= E_{\rm switch} + E_{\rm leak} \\ &= \frac{1}{2} nCV_{\rm dd}^2 \left[\alpha + \eta \cdot n \cdot e^{\left(-\frac{V_{\rm dd}}{mV_T}\right)}\right] \end{aligned} \tag{2}$$

where

μ	mobility;
$C_{\rm ox}$	oxide capacitance;
W	width;
L	length;
m	subthreshold slope factor;
V_T	thermal voltage;
$V_{\rm th}$	threshold voltage;
$V_{\rm gs}$	gate-source voltage;
$V_{\rm ds}$	drain-source voltage;
n	length of inverter chain;
η	fitting coefficient.

Operating CMOS circuits at $V_{\rm min}$ usually leads to large performance degradation. For example, recent publications show that microprocessors operate at clock frequencies of hundreds of kHz at 300–400 mV [4]–[7]. However many energy-constrained

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applications, such as biomedical and environmental sensor systems, have relaxed performance requirements [8]. Therefore, ultra-low $V_{\rm dd}$ operation represents a viable option for them.

Studies of ultra-low $V_{\rm dd}$ operation have been conducted at the technology, circuit, and architecture levels. At the technology level, the existing scaling strategies of modern CMOS that emphasize high performance can be sub-optimal for minimizing energy consumption in ultra-low $V_{\rm dd}$ regimes. Therefore, there have been proposals on new device designs [9], [10] as well as technology selection [11], [12] for ultra-low voltage operations. At the circuit level, design methodologies for better energy [13], variability [14], and performance [15], [16] have been investigated. In particular, static random access memory (SRAM) has been intensively studied, since the reduced on-current to off-current ratio degrades the robustness of back-to-back inverters in ultra-low $V_{\rm dd}$ regimes. To improve robustness, different bitcell topologies including 6T [17], [18], 8T [19], [20], 10T [21], and 12T [22] SRAM have been proposed to replace the conventional 6T. Research at the architecture level has focused on simple and energy-efficient architectures for ultra-low power microprocessors [36].

Ultra-low $V_{\rm dd}$ computational cores [4], [23] and general microprocessors [7], [25], [26] have been designed and tested showing that ultra-low $V_{\rm dd}$ designs achieve the active energy consumption of several pJ per cycle. However, these designs have often overlooked the importance of sleep energy consumption. Sleep energy, which has become important in modern CMOS processes due to the increasing contributions of subthreshold and gate leakage current, becomes more significant in ultra-low $V_{\rm dd}$ operations for two reasons. First, the reduced switching energy consumption from scaled supply voltages renders the sleep energy a more significant portion of total energy consumption. Second, ultra-low power applications often have low duty cycles. Although they run slowly at $V_{\rm min}$, there is a considerable amount of sleep time between the moment of completing a task ($T_{\rm min}$) and the start of a new task ($T_{\rm deadline}$), as defined in Fig. 2. Since there is a considerable amount of sleep energy consumption during the period, an optimization method that considers sleep energy consumption is vital to an energy-optimal design.

This paper extends one of the earliest works regarding sleep energy analysis and optimization in ultra-low $V_{\rm dd}$ regimes [28]. We start by proving the importance of sleep energy for reducing total energy consumption. Then, we discuss the effects of power gating switches (PGSs) [29], a well-known sleep energy reduction scheme, on energy consumption in ultra-low $V_{\rm dd}$ regimes. Our proposed optimization, which modulates PGS size and supply voltage simultaneously, suggests using very small PGSs with a supply voltage higher than $V_{\rm min}$, unlike conventional practices in which a large PGS is often used (typically $\sim$10% of total NFET width). In SPICE simulations of generic circuits, the optimization method achieves 125$\times$ reduction in total energy consumption and 50$\times$ savings in PGS area. The effectiveness of this proposed optimization is also confirmed by measurement results from a fabricated microprocessor. We also discuss the functional feasibility of using minimal PGSs with SPICE simulations and silicon measurements. Finally, other approaches to perform power gating are quantitatively compared for energy optimal designs.

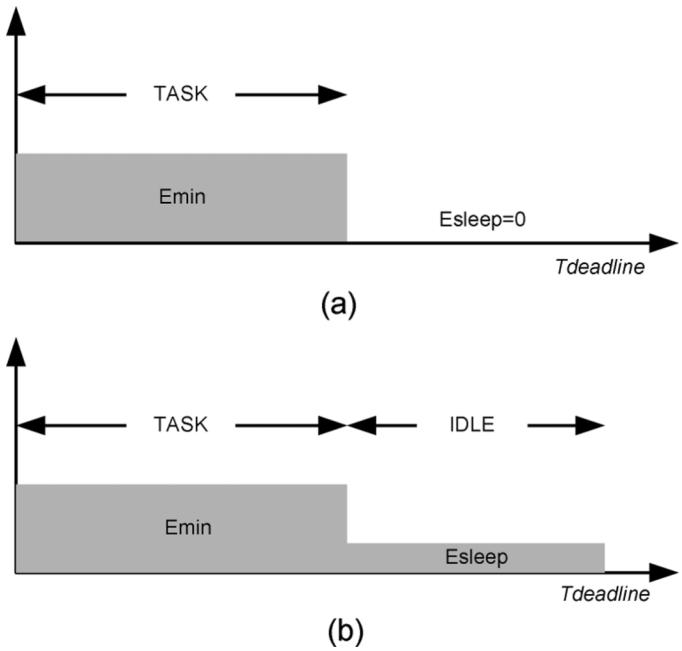

Fig. 2. Illustration of task scheduling at different deadlines. (a) Task is completed before $T_{\rm deadline}$ at $V_{\rm min}$, assuming only $E_{\rm min}$ consumed. (b) Task is completed before T deadline at $V_{\rm min}$, consuming $E_{\rm min} + E_{\rm sleep}$.

II. Impact of Sleep Energy on Total Energy Consumption

We first investigate the case in which circuits experience nonzero sleep time. In other words, $T_{\rm min}$, the time when circuits complete a task at the traditional $V_{\rm dd} = V_{\rm min}$ comes earlier than $T_{\rm deadline}$, the moment when the circuit begin a new task. In this case, the total energy is the sum of sleep energy ($E_{\rm sleep}$) and active energy ($E_{\rm switch} + E_{\rm leak}$). We define duty cycle $K_{\rm duty}$ as $T_{\rm deadline}/T_{\rm min}$, which represents the ratio of maximum allotted-time to actual used-time (i.e., circuit delay at $V_{\rm min}$). If $K_{\rm duty} > 1$, then circuits experience sleep time and consume additional energy.

For this scenario, we run SPICE simulations using inverter chains to estimate the contribution of sleep energy consumption to total energy consumption. In this paper, SPICE simulations are performed using a commercial 0.13-μm CMOS technology. Unless mentioned explicitly, a 99-stage inverter chain is used. Inverters use regular $V_{\rm th}$ devices while PGSs uses high $V_{\rm th}$ device. The $V_{\rm th,high-V_{th}}$ is $\sim$560 mV and $V_{\rm th,regular}$ is 350 mV at nominal conditions. At $V_{\rm dd}$ =$V_{\rm min}$ (220 mV), $E_{\rm min}$ of the inverter chain is simulated as 15.4 fJ/cycle at a delay of 5.66 μs (176 kHz). NFETs and PFETs in inverters are sized at 0.32 μm. Wiring parasitics are not included in simulations. The logic depth of the inverter chain is equivalent to 25 fan-out-of-4 (FO4) delays, which is shorter than most ultra-low $V_{\rm dd}$ designs. For a single inverter chain, the circuit activity rate is 1. The chosen logic depth and switching activity approximate the worst-case

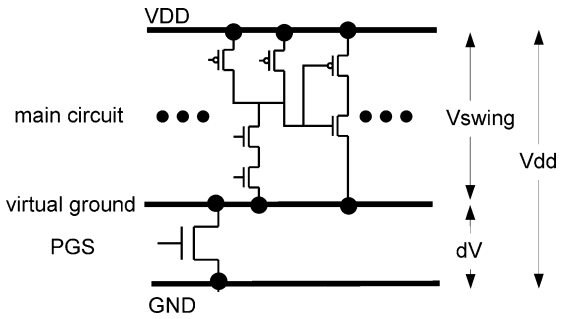

Fig. 3. Basic PGS configuration.

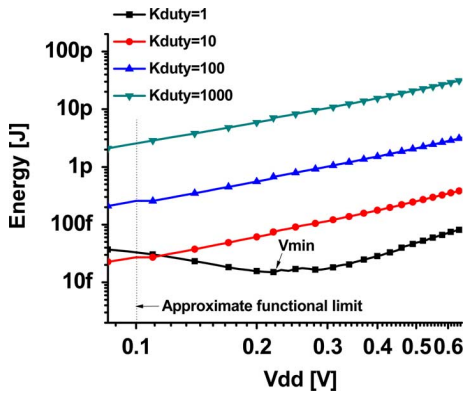

Fig. 4. $V_{\min}/E_{\min}$ curves with different K_{duty} considering sleep energy.

voltage drop scenario across power gating switches, and provide conservatism in the results.

We initially assume that there is no cutoff technique applied in sleep mode. The total energy consumption for inverter chains can be expressed as (3), which is derived from (2). Equation (3) shows that nearly the same amount of leakage current exists for both sleep and active time. Therefore, a significant increase in total energy consumption is expected. Fig. 4 shows that sleep energy contributes a large amount of energy consumption at lower duty cycles or higher K_{duty} (i.e., circuits spend more time in sleep mode). Since ultra-low power applications often have low duty cycles, it is paramount to consider sleep energy in total energy optimization frameworks

$$\begin{aligned} E_{\text{Total}} &= E_{\text{switch}} + E_{\text{leak}} + E_{\text{sleep}} \\ &= E_{\text{switch}} + t_{\text{delay}} P_{\text{leak}} + (T_{\text{deadline}} - t_{\text{delay}}) \cdot P_{\text{leak}} \\ &= E_{\text{switch}} + T_{\text{deadline}} P_{\text{leak}}. \end{aligned} \tag{3}$$

Another interesting observation is that both E_{switch} and $T_{\text{deadline}} \cdot P_{\text{leak}}$ in (3) are proportional to V_{dd}, resulting in lower energy-optimal supply voltage than conventional $V_{\min}$, as shown in Fig. 4. The optimal supply voltage can be scaled down until CMOS gates fail to function, while it is often bounded by the contribution of leakage energy in the conventional analysis. The minimal functional voltage for CMOS gates is assumed to be ~100 mV, although this assumption has little impact on the results of this work.

III. Effects of Cutoff Structures on Total Energy Consumption

Given the significant contribution of sleep energy to total energy consumption, PGSs are attractive for improving overall energy efficiency. While several other methods can be used in sleep mode, such as reverse body-biasing, PGSs are considered the most effective measure to reduce leakage energy consumption [37], [38]. However, PGS design in ultra-low V_{dd} regimes differs from conventional practices. Therefore, in this section, we first study the effects of PGSs on energy consumption of circuits operating in ultra-low voltage regimes. Section IV then lays out a strategy for using PGSs to minimize total energy consumption based on our findings in this section.

The purpose of employing PGSs in circuits is to reduce sleep power by strongly shutting off leakage paths during sleep modes. However, the benefit of reducing sleep energy consumption comes with performance degradation due to the voltage drop across PGSs [29]. In ultra-low voltage regimes, the performance degradation can induce extra active energy consumption since circuits consume extra leakage energy for longer periods of active time. Therefore, designers should be aware of the effects of PGSs on sleep and active energy consumption in ultra-low V_{dd} regimes.

To capture the effects of PGSs on energy consumption, we propose two parameters in (4). The first parameter, denoted by K_{leak}, sleep energy reduction factor, is the ratio of sleep power with PGSs to sleep power without such structures. The second parameter, the delay degradation factor, denoted by $1/K_{\text{delay}}$, is the ratio of circuit delay with PGSs to delay without them

$$\frac{1}{K_{\text{delay}}} = \frac{t_{\text{delay\_}w/\text{\_PGS}}}{t_{\text{delay\_}w/o\text{\_PGS}}} \quad K_{\text{leak}} = \frac{I_{\text{leak},w\text{\_PGS}}}{I_{\text{leak},w/o\text{\_PGS}}} \quad (0 < K_{\text{delay}},\ K_{\text{leak}} < 1). \tag{4}$$

A. Theoretical Power Gating Switch

This section investigates $E_{\min}$ assuming that circuits use a theoretical PGS having independent controls on K_{leak} and $1/K_{\text{delay}}$. For example, (5) shows the total energy consumption of circuits with the PGS of K_{leak} and $1/K_{\text{delay}}$, where $T_{\min}$ denotes the delay of main circuits at $V_{\min}$ without the PGS; P_{leak} denotes the leakage power without the PGS; and t_{delay} expresses the delay of main circuits at a specific V_{dd} with the PGS. In (5), E_{switch} is technically affected by the PGS due to the change of the voltage swing. However, this can be ignored without sacrificing much accuracy. However, we include the changes of E_{switch} after this section for a more complete analysis

$$\begin{aligned} E_{\text{Total}} &= E_{\text{switch}} + E_{\text{leak}} + E_{\text{sleep}} \\ &= E_{\text{switch}} + \frac{1}{K_{\text{delay}}} t_{\text{delay}} P_{\text{leak}} \\ &\quad + \left(K_{\text{duty}} T_{\min} - \frac{1}{K_{\text{delay}}} t_{\text{delay}} \right) \cdot K_{\text{leak}} P_{\text{leak}} \end{aligned} \tag{5}$$

where t_{delay} is delay of circuits without PGSs and $T_{\min}$ is delay of circuits at $V_{\min}$ without PGSs

We investigate the changes of $V_{\min}$ and $E_{\min}$ while sweeping either K_{leak}, as shown in Fig. 5(a) and (b), or $1/K_{\text{delay}}$ as shown

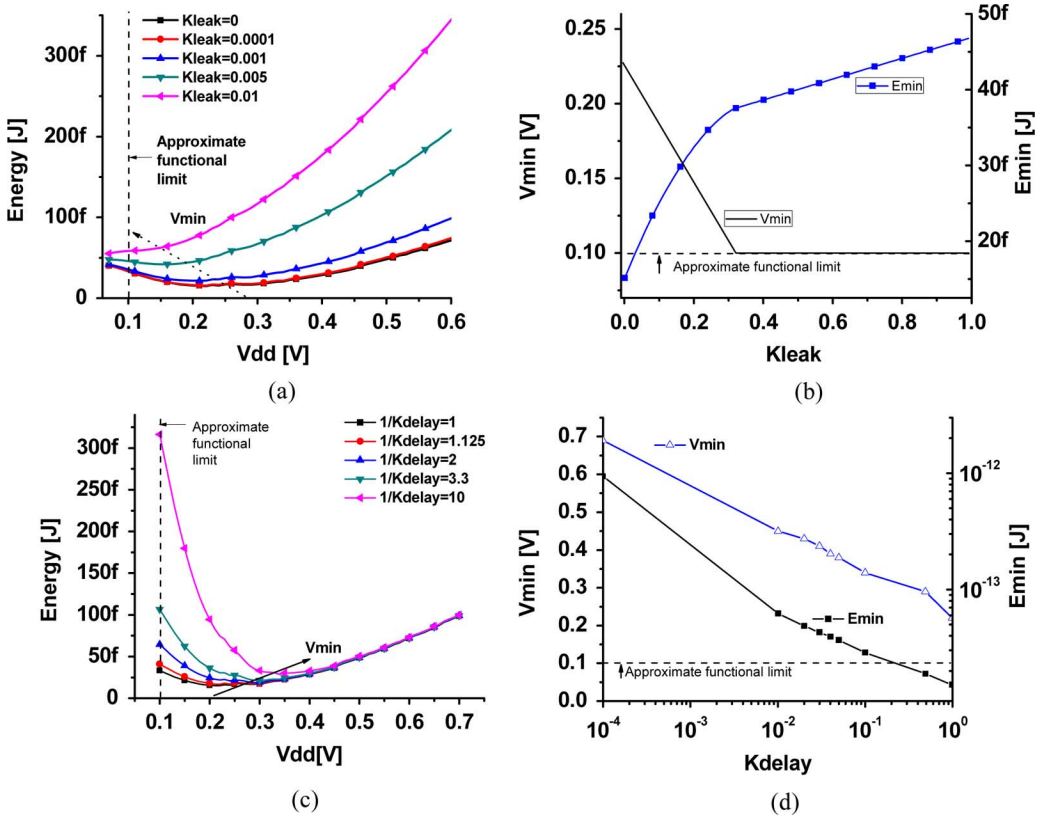

Fig. 5. $V_{\min}/E_{\min}$ change with K_{leak} and K_{delay}. (a) $V_{\min}/E_{\min}$ curves. (b) $K_{\text{leak}} - V_{\min}/E_{\min}$. (c) $V_{\min}/E_{\min}$ curves. (d) $K_{\text{delay}} - V_{\min}/E_{\min}$.

in Fig. 5(c) and (d). Fig. 5(a) and (b) show that small values of K_{leak} can reduce E_{sleep} and push $V_{\min}$ to a conventional $V_{\min}$. On the other hand, Fig. 5(c) and (d) show that large values of $1/K_{\text{delay}}$ increases E_{leak} due to the longer delay. Since higher V_{dd} can alleviate the performance degradation, higher $V_{\min}$ is preferred to offset the increase of E_{leak} for this case.

B. Practical Power Gating Switch

While we assume PGSs with independent controls on K_{leak} and $1/K_{\text{delay}}$ in the previous section, they are actually corelated in practical PGS designs. For a simple PGS (see Fig. 3), we can derive $1/K_{\text{delay}}$ and K_{leak} in ultra-low V_{dd} regimes, as shown in (6) and (7). In the derivation, it is assumed that the voltage across the PGS in sleep mode is $\sim V_{\text{dd}}$, due to the very high resistance of the PGS when it is off. V_{swing}, which is a highly nonlinear function of PGS width and technology parameters, reduces for wider PGSs and lower threshold voltages

$$\begin{aligned}\frac{1}{K_{\text{delay}}} &= \frac{t_{\text{delay\_}w/\text{\_PGS}}}{t_{\text{delay\_}w/o\_PGS}} \\ &= \frac{CV_{\text{swing}}}{CV_{\text{dd}}} \\ &\quad \cdot \frac{\mu_{\text{main}} C_{\text{ox}} \frac{W}{L} V_T^2 (m-1) e^{\frac{-V_{\text{swing}}}{mV_T}} \left(1 - e^{\frac{-V_{\text{swing}}}{mV_T}}\right)}{\mu_{\text{main}} C_{\text{ox}} \frac{W}{L} V_T^2 (m-1) e^{\frac{-V_{\text{dd}}}{mV_T}} \left(1 - e^{\frac{-V_{\text{dd}}}{mV_T}}\right)} \\ &= \frac{V_{\text{swing}}}{V_{\text{dd}}} e^{\frac{V_{\text{dd}} - V_{\text{swing}}}{mV_T}} \end{aligned} \tag{6}$$

$$\begin{aligned}K_{\text{leak}} &= \frac{I_{\text{leak\_}w/\text{\_PGS}}}{I_{\text{leak\_}w/o\text{\_PGS}}} \\ &= \frac{\mu_{\text{PGS}} C_{\text{ox}} \frac{W_{\text{PGS}}}{L_{\text{PGS}}} \exp\left(\frac{-V_{th\_\text{PGS}}}{mV_T}\right) \left(1 - \exp\left(-\frac{V_{\text{dd}}}{V_T}\right)\right)}{\mu_{\text{main}} C_{\text{ox}} \frac{W_{\text{main}}}{L_{\text{main}}} \exp\left(\frac{-V_{th\_\text{main}}}{mV_T}\right) \left(1 - \exp\left(-\frac{V_{\text{dd}}}{V_T}\right)\right)} \\ &= k \cdot W_{\text{PGS}} \end{aligned} \tag{7}$$

where

V_{swing}	voltage swing without voltage drop in PGSs;
μ	mobility;
C_{ox}	oxide capacitance;
W	width;
L	length;
m	subthreshold slope factor;
V_T	thermal voltage;
V_{th}	threshold voltage;
V_{dd}	supply voltage.

Both $1/K_{\text{delay}}$ and K_{leak} are functions of PGS width and supply voltage, as shown in (6) and (7). $1/K_{\text{delay}}$ can quickly approach 1 by increasing the width of PGSs at high supply voltages, while it slowly increases at low supply voltages. On the other hand, K_{leak} is a linear function of the width of PGSs at a wide range of supply voltages. Fig. 6(a) and (b) compare the derived equations against SPICE simulations, demonstrating acceptable accuracy. Fig. 6(c) shows the inter-relationship between K_{leak} and $1/K_{\text{delay}}$ as the width of PGSs is swept. The

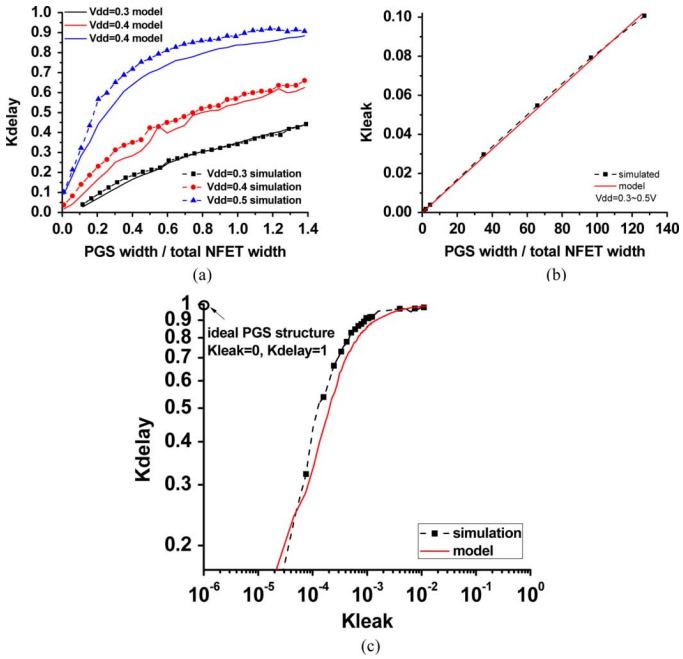

Fig. 6. K_{leak} and K_{delay} change with PGS width and V_{dd}. (a) width—K_{delay}. (b) width—K_{leak}. (c) $K_{\text{leak}} - K_{\text{delay}}$.

ideal cutoff structure point is at the point where $K_{\text{leak}} = 0$ and $1/K_{\text{delay}} = 1$. This figure also provides a means to quantitatively compare the efficacy of different PGSs for ultra-low V_{dd} regimes, as discussed further in Section VI.

As shown in (8), total energy consumption can be derived from (5)–(7). The change of E_{switch} from PGS is included here for higher accuracy. Equation (8) shows that the total energy is a function of V_{dd}, K_{leak}, K_{delay}, and technology parameters. T_{min} is the circuit delay without PGSs evaluated at its own V_{min}, and is thus constant

$$\begin{aligned} E_{\text{Total}} &= E_{\text{switch}} + E_{\text{leak}} + E_{\text{sleep}} \\ &= \frac{1}{2} \cdot n \cdot C V_{\text{dd}} V_{\text{swing}} \cdot \alpha \\ &\quad + \frac{1}{2} n C V_{\text{dd}}^2 \eta \cdot n e^{\frac{-V_{\text{dd}}}{mV_T}} \cdot \left(\frac{V_{\text{swing}}}{V_{\text{dd}}} e^{\frac{V_{\text{dd}} - V_{\text{swing}}}{mV_T}} \right) \\ &\quad + \left(K_{\text{duty}} T_{\text{min}} - e^{\frac{V_{\text{dd}} - V_{\text{swing}}}{mV_T}} \cdot t_{\text{delay}} \right) \\ &\quad \cdot k \cdot W_{\text{PGS}} \cdot I_{\text{leak\_}w/o\_\text{PGS}} V_{\text{dd}} \\ E_{\text{Total}} &\approx K_1 V_{\text{dd}} V_{\text{swing}} + K_2 V_{\text{dd}}^2 e^{\frac{-V_{\text{dd}}}{mV_T}} \\ &\quad \times \left(\frac{V_{\text{swing}}}{V_{\text{dd}}} e^{\frac{V_{\text{dd}} - V_{\text{swing}}}{mV_T}} \right) + K_3 K_{\text{duty}} W_{\text{PGS}} V_{\text{dd}} \end{aligned} \tag{8}$$

where

n	length of inverter chain;
C	capacitance per inverter
α	activity factor;
V_{swing}	voltage swing without voltage drop in PGSs;
η	fitting coefficienct;
V_{dd}	supply voltage;

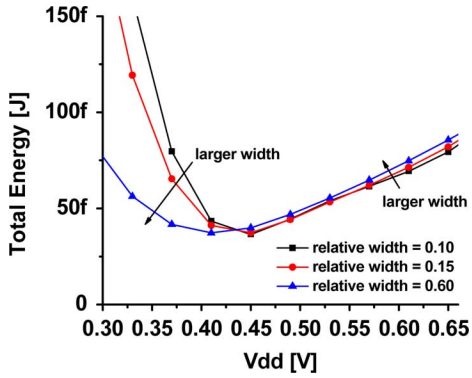

Fig. 7. $V_{\text{min}}/E_{\text{min}}$ with different PGS sizes $K_{\text{duty}} = 100$.

T_{min}	delay of inverter chain without PGSs at original V_{min};
m	subthreshold slope factor;
t_{delay}	delay of inverter chain without PGSs;
k	fitting coefficient from (7);
V_T	thermal voltage.

Since K_{leak} and K_{delay} are functions of supply voltage and PGS width, we investigate energy consumption by sweeping both of these parameters. Sleep energy consumption is roughly proportional to both supply voltage and PGS width. Here, the effect of t_{delay} on sleep energy consumption is ignored since for large K_{duty} the t_{delay} term in E_{sleep} is much smaller than $K_{\text{duty}} \times T_{\text{min}}$ while for small K_{duty} the sleep energy consumption itself becomes small and less important in E_{total}. Additionally, subthreshold leakage current, the dominant source of sleep energy consumption, is nearly constant with supply voltage in the ultra-low V_{dd} regime while it often increases in super-threshold regimes due to short-channel effects. Therefore, we use a lumped coefficient, K_3, for simplicity in (8).

On the other hand, active energy consumption has a complex relationship with supply voltage and PGS width. First, PGS width affects the performance of circuits. For example, small PGSs (i.e., larger $1/K_{\text{delay}}$) induce longer delay, resulting in higher E_{leak} consumption in circuits. In near-threshold regimes ($V_{\text{dd}} > 450$ mV for this technology), the increase in E_{leak} is relatively small, while it can significantly increase total energy consumption in sub-threshold regimes due to the importance of E_{leak}, as shown in Fig. 7.

The effect of supply voltage on active energy consumption is similar to the traditional analysis [3]. Lowing V_{dd} causes performance degradation and thus leads to higher E_{leak} consumption (i.e., higher $1/K_{\text{delay}}$), while it quadratically reduces E_{switch}.

One interesting observation is that large values of $1/K_{\text{delay}}$ or E_{leak} can be alleviated by either using larger PGSs or raising supply voltages. However there is a difference between these approaches. Using larger PGSs reduces the voltage drop across PGSs, leading to lower active energy consumption compared to raising supply voltage. However, raising supply voltage is more effective in improving performance with a smaller increase in sleep energy consumption. To confirm these trends, we perform SPICE simulations where circuits initially have excessive E_{leak} consumption that must be alleviated using either of the

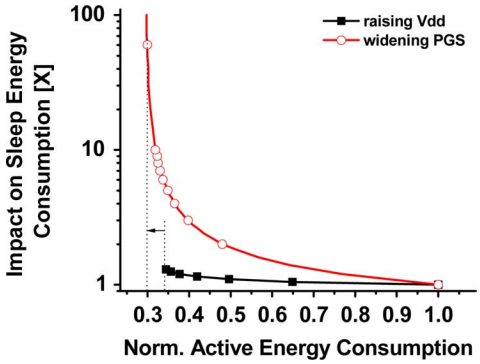

Fig. 8. Comparison between raising V_{dd} and upsizing PGS in energy optimization.

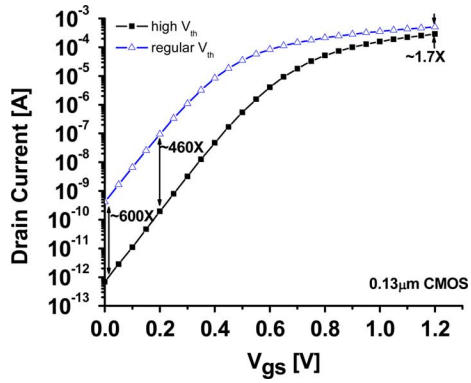

Fig. 9. On/off-current of high $V_{\rm th}$ and regular $V_{\rm th}$ devices.

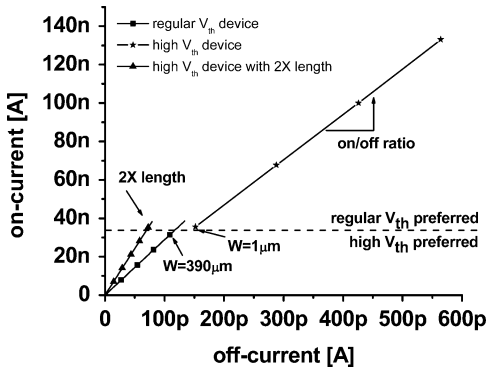

Fig. 10. Off-current versus on-current as sweeping PGS width.

discussed methods. Fig. 8 shows that both raising $V_{\rm dd}$ and widening PGS can reduce active energy consumption but with differing impacts on sleep energy consumption. The larger PGS increases sleep energy consumption by 30× while raising supply voltage incurs only a 25% penalty. Given the advantage of widening PGS is improved active energy consumption compared to raising $V_{\rm dd}$, this approach should be used in cases of small $K_{\rm duty}$, where active energy is more important than $E_{\rm sleep}$, which will be confirmed in Section IV-A.

IV. Strategy of Using Power Gating Switches in Ultra-Low $V_{\rm dd}$ Regimes

A. PGS Design Strategies in Ultra-Low $V_{\rm dd}$ Regimes

This section presents a strategy for using PGSs in ultra-low $V_{\rm dd}$ regimes based on the findings in Section III. We first review the conventional methods of designing PGSs. Then, we propose our PGS design method employing cooptimization in ultra-low $V_{\rm dd}$ regimes. In this method, supply voltage and PGS width are simultaneously chosen to achieve full energy savings at a given duty cycle.

For the designs targeted at nominal $V_{\rm dd}$ operations the performance degradation is often constrained by less than 5%–10%. Therefore, the width of PGSs needs to be large enough to supply proper current and minimize virtual ground bounces. Often, the constraints lead to large PGS width, often ∼10% of total NFET width of main circuits [29], [30].

Also, high $V_{\rm th}$ devices have been a popular choice for PGSs since they have similar on-current but much smaller off-current than regular $V_{\rm th}$ devices. Fig. 9 shows that in this technology, high $V_{\rm th}$ devices have 600× smaller off-current, while they have only 1.7× smaller on-current at $V_{\rm dd} = 1.2$ V. Therefore, high $V_{\rm th}$ PGSs can provide ∼352× reduction in off-current at the same on-current.

In ultra-low $V_{\rm dd}$ regimes, PGS design can be different. High $V_{\rm th}$ devices become less attractive since they have the similar on-current to off-current ratio as regular $V_{\rm th}$ devices in ultra-low $V_{\rm dd}$ regimes. Here on-current is defined as saturation current since the $V_{\rm ds}$ required for device saturation is only 3–4V_T in ultra-low $V_{\rm dd}$ regime. Using high $V_{\rm th}$ PGSs is beneficial only for the case where circuits draw a current smaller than what a minimum-sized regular $V_{\rm th}$ PGS can deliver. Fig. 10 shows that circuits with current of less than ∼30 nA can exploit high $V_{\rm th}$ PGSs for the targeted technology. For the higher current draw, regular $V_{\rm th}$ devices are preferred due to an unnecessary use of area by high $V_{\rm th}$ PGSs. The crossover point between regular $V_{\rm th}$ and high $V_{\rm th}$ PGS is technology-dependent, thus requiring careful evaluations for each technology.

In this sense, devices with a large on-current to off-current ratio are preferred for PGSs in ultra-low $V_{\rm dd}$ regimes. One way of improving the ratio is to use longer channel devices [16], as shown in Fig. 10. Note that in this particular technology, high $V_{\rm th}$ devices exhibit a slightly better on-current to off-current ratio than regular $V_{\rm th}$ devices. However, since the ratio is technology-dependent, a careful evaluation is needed for each technology.

Another important factor to consider is that the conventional practices of sizing PGSs for maintaining performance is no longer valid since minimizing total energy consumption is a more important goal for ultra-low power applications. Therefore, PGSs should be optimized for minimizing total energy consumption. Since both PGS width and supply voltage affect total energy consumption, as we discuss in Section III, we propose an optimization method, called cooptimization, for designing PGSs. In this proposed method, PGS width and supply voltage are simultaneously selected for minimizing total energy consumption.

We investigate total energy consumption at different duty cycles by sweeping all combinations of PGS widths and supply voltages in the SPICE simulations using inverter chains. If $K_{\rm duty}$ is equal to one, then the optimal energy consumption can be achieved by supplying the conventional $V_{\rm min}$ without

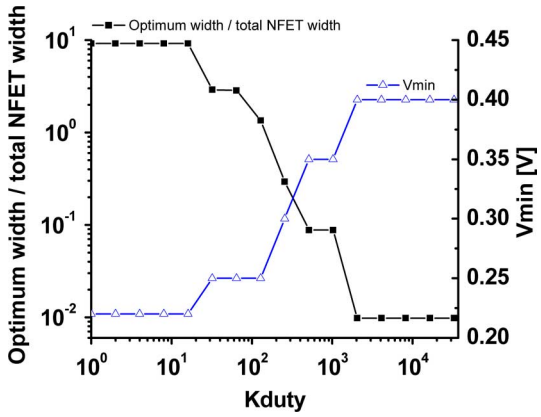

Fig. 11. New $V_{\min}$ and optimal PGS size at different K_{duty}.

PGSs. This is because PGSs induce extra delay and more E_{leak} consumption. Since there is no sleep time, i.e., $K_{\text{duty}} = 1$, the sleep leakage reduction is of no use in this case. The results are shown at the left end of Fig. 11.

When K_{duty} falls roughly between 1 and 100, the optimal V_{dd} is similar to the conventional $V_{\min}$ and the optimal PGS width becomes large. These relatively small values of K_{duty} imply that E_{sleep} is small. Therefore, the increase in E_{sleep} caused by the use of larger PGSs is a negligible part of total energy consumption. This is well matched to the idea expressed in Section III, that increasing PGS width is more energy-efficient than raising V_{dd} when sleep time is small. This is well supported by SPICE simulations using inverter chains, as shown in Fig. 11. If the large PGS causes too much area overhead, it can be omitted with a relatively small sleep energy penalty.

When $K_{\text{duty}} > 100$, small PGSs and $V_{\text{dd}} > V_{\min}$ are preferred for minimizing total energy consumption since raising V_{dd} imposes a lower penalty on E_{sleep}, as discussed in Section III. This is confirmed by SPICE simulations using inverter chains, as shown in Fig. 11. The small PGSs force the effective voltage between virtual rails to approach conventional $V_{\min}$.

Typical sensor-type applications have K_{duty} of $\sim 10^4$ [8]. Therefore, to achieve optimal energy consumption, the regular V_{th} PGS can be downsized to 0.01% of total NFET width of main circuits, as shown in Fig. 11. However, since 0.01% of total NFET width is smaller than the minimum width of device in this technology, a high V_{th} PGS is instead used. For the same on-current, the high V_{th} PGS should be sized at 1% of total NFET width of the main circuits.

As stated earlier the logic depth and switching activity of the test circuits incur worst-case voltage drop across PGSs. Since higher logic depth or less activity reduces the current delivery requirement, optimized PGSs can be made even smaller in many practical settings. As a reference data point, the cooptimization for an inverter chain with 2× logic depth and 1/2 the activity factor relative to the baseline system of this work suggests the use of a 50% smaller PGS at 25 mV higher V_{dd} for $K_{\text{duty}} = 10^4$ to achieve optimal energy consumption. The smaller voltage glitch on the virtual ground rail allows further scaling of PGS size while the lower circuit switching activity increases $V_{\min}$

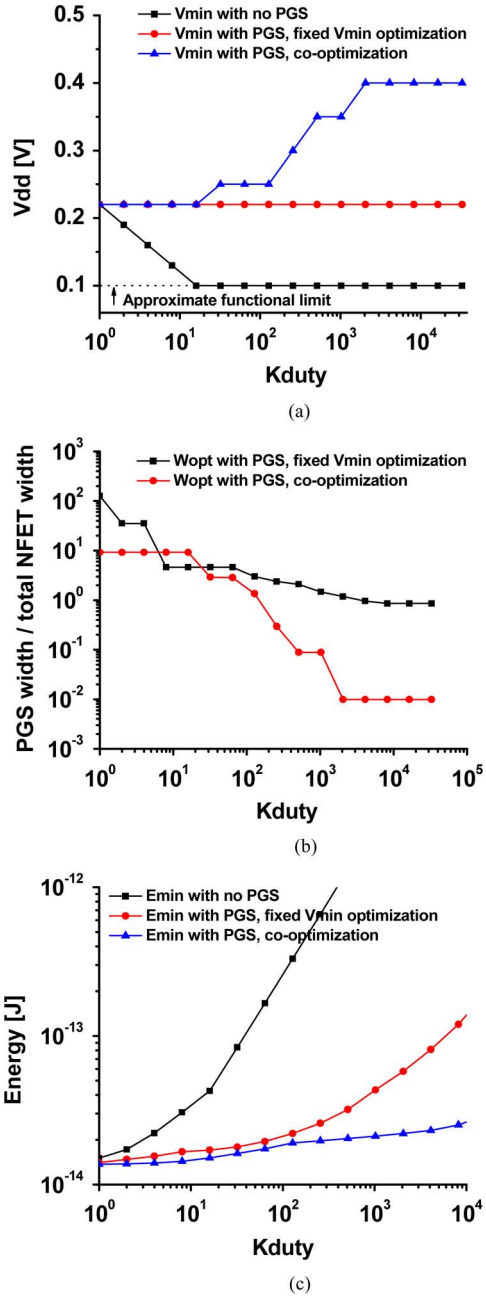

Fig. 12. Comparison of three optimization strategies. (a) $K_{\text{duty}} - V_{\min}$ over three strategies. (b) K_{duty}—optimal PGS width over three strategies. (c) $K_{\text{duty}} - E_{\min}$ over three strategies.

due to a larger leakage to dynamic energy ratio. Baseline PGS size and V_{dd} settings incur a 6.7% energy penalty in this longer and lower activity circuit rather than its optimal values.

B. *Comparisons of the Optimization Methods*

We run SPICE simulations using inverter chains to compare our proposed cooptimization with two baseline approaches for designing PGSs. The first baseline approach is to use no cutoff structure and optimize supply voltage only. The second baseline approach, referred to as fixed-$V_{\min}$-optimization, uses PGSs at a conventional fixed $V_{\min}$. Wiring parasitics are not included in simulations. Fig. 12(a) shows the change of $V_{\min}$ for each strategy. It illustrates that the cooptimization calls for a higher

$V_{\rm dd}$ than the conventional $V_{\rm min}$ for large values of $K_{\rm duty}$. However, the $V_{\rm min}$ is scaled down to the functional limit of supply voltage that allows the task to be completed in a given time $(K_{\rm duty})$ for the no-cutoff approach.

On the other hand, Fig. 12(b) illustrates the optimal PGS width for each optimization approach. The cooptimization suggests the use of extremely small PGSs for energy optimization. However, the fixed-$V_{\rm min}$-optimization cannot suggest such small PGSs since they degrade performance and thus consume extra active energy at the fixed $V_{\rm min}$.

Finally, the total energy consumption of these strategies is compared in Fig. 12(c). Even at relatively small values of $K_{\rm duty}$, the no-cutoff strategy consumes a significantly large amount of energy. The fixed-$V_{\rm min}$ optimization and cooptimization exhibit comparable energy consumption for small values of $K_{\rm duty}$. However, cooptimization saves a considerable amount of total energy consumption when $K_{\rm duty} > 1000$. Note that sensor applications often have $K_{\rm duty}$ larger than 1000. For these high $K_{\rm duty}$ applications, the cooptimization can save up to $\sim$99% of total energy consumption, compared to the other approaches.

C. Case Study Using a Fabricated Microprocessor

We apply the proposed design method to a microprocessor designed for ultra-low power applications [26]. It is fabricated in 0.18-μm CMOS and consists of $\sim$4000 gates. The total NFET width is $\sim$6000 μm. The microprocessor has tunable PGSs with widths ranging from 0.66 to 28 μm for mitigating the effects of process variations on PGSs. Using the smallest PGS, $E_{\rm active}$ is measured as 2.35 pJ/cycle with $I_{\rm sleep} = 2$ pA. The processor operates at 60 kHz with $V_{\rm dd} = 0.475$ V. For the smallest and the largest PGSs, we measure active energy consumption and sleep energy consumption. We estimate that 1000 instructions are executed during active mode. We then calculate the total energy consumption at several values of $K_{\rm duty}$.

Fig. 13 shows that as sleep time become small (i.e., larger $K_{\rm duty}$) the ideal strategy transitions from using the widest (28 μm) PGS to employing the 0.66 μm PGS. The large PGS is slightly more energy efficient at high duty cycles due to less performance degradation and smaller voltage drop across the PGS. However, the small PGS becomes energy-optimal at low duty cycles since sleep energy consumption represents a large portion of total energy consumption. These strategies cross over when $T_{\rm deadline}$ is 4 s. Since $T_{\rm deadline}$ for most ultra-low power systems is larger than 4 s [8], small PGSs are energy-optimal for these applications. If 1000 s (16 min) sleep time is assumed, the small PGS provides 4.6$\times$ lower total microprocessor energy consumption compared to the large PGS. We cannot measure $T_{\rm min}$ of the microcontroller (i.e., the microprocessor delay at $V_{\rm min}$ without PGSs), therefore we approximate it as the delay at $V_{\rm min}$ with the large PGS. With the estimated $T_{\rm min}$, the $K_{\rm duty}$ for 10 s is $\sim 10^6$.

V. Feasibility of Minimal-Sized PGSs in Ultra-Low $V_{\rm DD}$ Regimes

Even if performance degradation is ignored, designers are unlikely to view extremely small PGSs as viable options since the voltage drop across PGSs may cause functional robustness problems. In super-threshold regimes, it is true that the small PGSs cause functional failures. Fig. 14 shows that the microprocessor discussed in Section IV is not functional with the small PGSs at $V_{\rm dd} > 0.8$ V. However, in ultra-low $V_{\rm dd}$ regimes, the microprocessor with the small PGSs is functional. Therefore, it is important to understand the different feasibilities of small PGSs in ultra-low $V_{\rm dd}$ regimes.

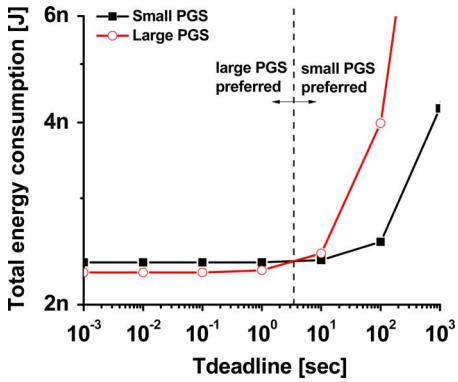

Fig. 13. Measured total energy consumption with two different PGS sizes from a test microprocessor.

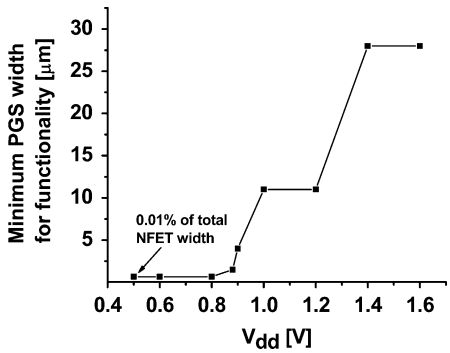

Fig. 14. Measured minimal PGS size for functionality.

One reason that the small PGS functions well in ultra-low $V_{\rm dd}$ regimes can be found in the relationship of $V_{\rm ds}$ and subthreshold current. As shown in (1), subthreshold current becomes insensitive to $V_{\rm ds}$ once $V_{\rm ds}$ is larger than 3–4$V_{\rm T}$. In other words, even if the microprocessor attempts to draw a large current, for example, because of many simultaneous internal node switches, the $V_{\rm ds}$ or voltage drop across the PGS changes only by a small amount. Instead, the current draw is limited and the microprocessor is slowed. However, linear and saturated current of devices in super-threshold regimes have a linear relationship with $V_{\rm ds}$. Therefore, the $V_{\rm ds}$ of the PGS quickly rises to the point at which the PGS can supply a large current. This $V_{\rm ds}$ increase appears as a large virtual ground bounce, making the minimal PGS less robust in super-threshold regimes.

To confirm these concepts, we perform SPICE simulations with two different sets of inverter chains. The first set has one inverter chain that is switching and four chains that are not switching. The second set has five inverter chains that are switching. Each inverter chain is identical, thus the second set draws $\sim 5\times$ higher current draw. We investigate voltage drops across PGSs for these circuits PGSs are sized at 0.05% of total NFET width for each set. Wiring parasitics are not included in simulations.

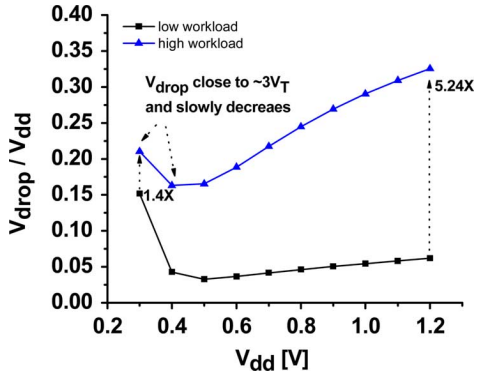

Fig. 15. Simulated virtual ground level over different workload and supply voltage.

Fig. 15 illustrates that relative virtual ground levels are smaller for ultra-low $V_{\rm dd}$ regimes for both low and high work load cases, which is expected, given the different relationships of $V_{\rm ds}$ with drain current in two different $V_{\rm dd}$ regimes. Additionally, in ultra-low $V_{\rm dd}$ regimes, the relative increase of the virtual ground level from low to high work load is smaller. The final observation is that the relative virtual ground level goes up at $V_{\rm dd} < 0.4$ V. This is because the $V_{\rm ds}$ of the PGS gets close to 3–4$V_{\rm T}$ and then decreases only slightly.

The 0.13- and 0.18-μm technologies considered in this paper exhibit less process variations than leading-edge scaled technologies. In such cases robustness can be improved by using a wider PGS at the cost of sleep energy consumption [37]. To further mitigate process variations, trimmable PGSs such as those in [26] can be used for selecting appropriate width PGSs post-silicon to minimize sleep energy. Since robust operation is of critical importance, statistical simulations across PVT (process, voltage, and temperature) variations should be considered.

VI. Beyond Basic PGSs

So far, we have discussed only the basic PGS topology. However there are many variations for PGSs to improve the fundamental tradeoff between performance degradation and sleep energy reduction. In this section, we quantitatively compare different flavors of PGSs and provide guidelines for choosing energy-optimal PGSs in ultra-low $V_{\rm dd}$ regimes.

Fig. 16 shows three well-known PGS topologies: basic PGS, DTCMOS PGS, and stack-forcing PGS. In DTCMOS PGSs, the gate and the body of the PGSs are tied to increase on-current. Therefore, DTCMOS PGSs are expected to have a smaller $1/K_{\rm delay}$, compared to the basic PGS. The stack-forcing PGS uses two FETs in series to reduce off-current using the stack effect [34]. These series-connected FETs induce negative $V_{\rm gs}$ at the upper FET, which exponentially decreases off-current. Therefore, it exhibits smaller $K_{\rm leak}$ than the basic PGS. However, $1/K_{\rm delay}$ can be worse. At $V_{\rm dd} = 0.5$ V, the $K_{\rm leak} - K_{\rm delay}$ curves of these structures are shown in Fig. 17. For the same $K_{\rm leak}$, the DTCMOS structure provides the smallest $1/K_{\rm delay}$, and thus the smallest $E_{\rm leak}$, followed by stack-forcing PGS.

Super-cutoff PGS [32] is not considered in comparisons since the penalty of generating bias voltages is difficult to quantify.

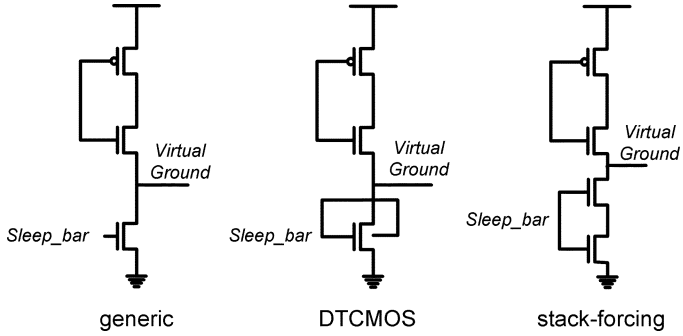

Fig. 16. Generic, DTCMOS, and stack-forcing PGS.

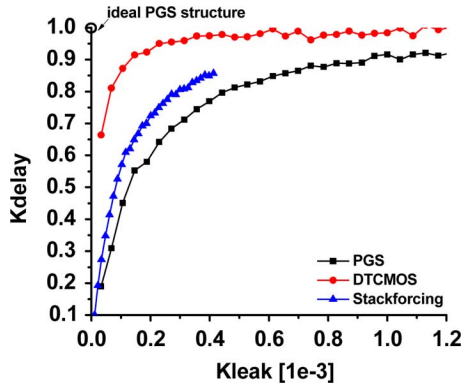

Fig. 17. $K_{\rm leak} - K_{\rm delay}$ curves with different PGSs.

However, it can be a promising design choice due to the exponential relationship between subthreshold current and supply voltage in ultra-low $V_{\rm dd}$ regimes. In [35], a detailed analysis on the tradeoff between generating bias voltages and sleep energy reduction is presented for ultra-low $V_{\rm dd}$ operations.

VII. Conclusion

This paper investigates the interaction of optimal energy, supply voltage, and PGS for ultra-low $V_{\rm dd}$ designs. The results show that ignoring sleep leakage energy in ultra-low $V_{\rm dd}$ regimes can significantly degrade energy efficiency. Therefore, we propose several approaches for designing PGSs including cooptimization, which seeks to achieve optimal energy by simultaneously adjusting both PGS size and $V_{\rm dd}$. Unlike typical practices in higher $V_{\rm dd}$ regimes, in which large PGSs and nominal supply voltage are often chosen, our proposed optimization suggests using minimal PGS and higher $V_{\rm dd}$ for those applications with long sleep time. This reduces energy by 125$\times$ in SPICE simulations. The effectiveness of the proposed method is confirmed by the silicon measurements from an ultra-low power microprocessor. Finally, the feasibility of using minimal-sized PGSs in ultra-low $V_{\rm dd}$ regimes is studied with the focus of functional robustness using SPICE simulations and silicon measurements.

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