

915MHz Ultra Low Power Receiver using Sub-V_t Active Rectifiers

Nathan E. Roberts, David. D. Wentzloff

University of Michigan, Ann Arbor, MI, USA

[nerobert,wentzlof]@umich.edu

A 98nW receiver with a 23nW active rectifier RF front-end biased in deep subthreshold near the saturation/linear boundary is presented. An on-chip voltage reference and 28nW hysteretic comparator are also designed using subthreshold techniques. The receiver can demodulate an OOK signal at 100kbps with a sensitivity of -41dBm and all processing for process and mismatch is handled on-chip [1]. The ultra-low power receiver is used for wireless sensor node applications, specifically for nodes that are to be worn on the body.

I. INTRODUCTION

Wireless sensor nodes are the next step in the continued evolution of computers, following Bell's Law which predicts a new class of computers about every decade. For wireless sensor nodes, the small form factor plays a significant role in design decisions and requires a very small battery or no battery at all. In order to effectively process and communicate sensory information under severe energy limitations, subthreshold-based circuit design has become an increasingly popular means of achieving energy efficient sensor nodes.

Wireless communication circuits are the energy bottleneck in sensor nodes. Focusing on receivers in particular, the energy is a result from the need to actively listen for packets and therefore not enter sleep mode, as well as the need for RF transconductance to amplify a small received signal. One well-known technique to improve energy consumption is through the use of an ultra-low power receiver that stays active while listening for packets while the main communication receiver is in sleep mode. Once the ultra-low power receiver receives a packet it wakes up the communication receiver. Publications show the power of this low power receiver to be around 50 μ W [2],[3]. For many energy constrained systems, like body worn sensor nodes, 50 μ W active power is still too high.

The receiver described in this paper has an active power consumption of 98nW, a sensitivity of -41dBm, and a data rate of 100kbps. Section II will describe the architecture and overall operation of our ultra-low power receiver and Section III will discuss the circuits that use subthreshold design. Section IV will discuss mismatch compensation and Section V will discuss measured results. Section VI concludes the paper.

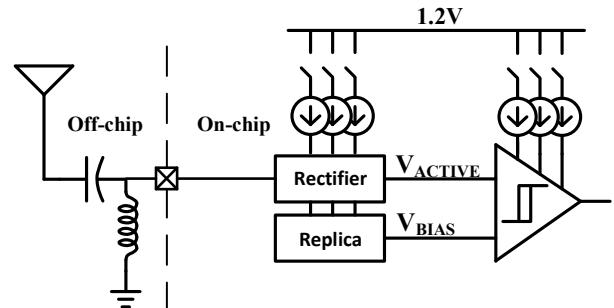


Figure 1. Block Diagram of Receiver

II. ULTRA-LOW POWER RECEIVER ARCHITECTURE

Subthreshold based rectifier architectures are a popular choice for low power radio design due to their simplicity and low power requirements. In order to be effective RF demodulators, rectifiers need large signals for maximum conversion gain efficiency, which typically means RF transconductance is required. Instead of RF transconductance, this receiver will utilize sensitivity reduction [4]. In addition, enough power is required to ensure fast response time. This receiver will reduce power by optimizing the bias point in the rectifier to ensure sufficient response time at reduced power levels.

Looking at Figure 1, a 915MHz OOK modulated signal is received at the input to the antenna at a rate of 100kbps. The input signal is boosted by around 10dB by the off-chip

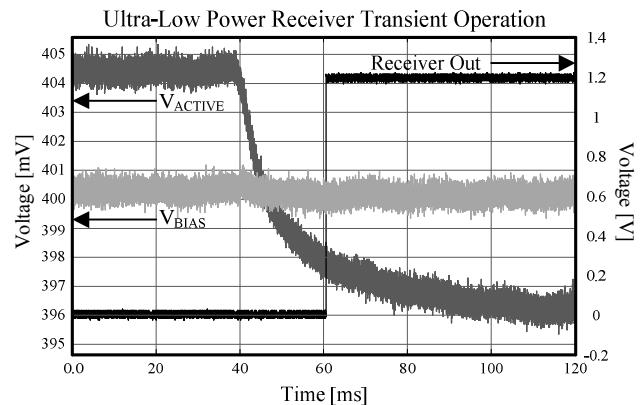


Figure 2. Measured Transient operation

matching network before going on-chip to the gate of the active rectifier. In the presence of a signal, the active

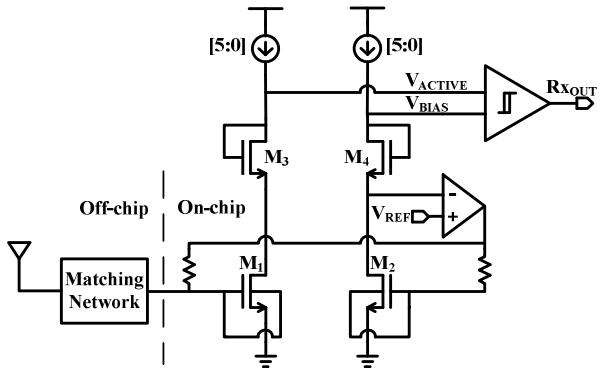


Figure 3. Sub- V_t Rectifier

rectifier's output voltage, V_{active} , will drop while the voltage of a replica bias rectifier, V_{bias} , will remain constant. The comparator will then toggle the output of the receiver. Figure 2 shows a measured transient of the receiver's operation.

III. SUBTHRESHOLD CIRCUITS

A. 23nW Self-Biased Rectifier

The rectifier, shown in Figure 3 in context with the rest of the receiver, is the RF front-end and therefore its design is critical to overall performance. It has to be sensitive enough to detect -40dBm signals, but also fast enough to demodulate the signal at 100kbps, all within a nano-watt power budget.

The 23nW rectifier begins with a DTMOS [5] common-source connected device, M_1 , in series with a diode-connected device, M_3 , with a current DAC on top. M_3 acts as a level shifter so the output of the active rectifier falls within the dynamic range of the comparator. The series connection of M_1 , M_3 , and the current DAC is then mirrored to create a replica bias (M_2 and M_4). Without an input signal connected to the replica bias, the output voltage will remain stable. The drain voltage of M_2 is sensed and compared with an on-chip voltage reference which is then used in feedback to bias M_2 's gate. This bias voltage is then fed forward to M_1 .

The design of the rectifier self-biases M_1 in deep subthreshold. Because a MOSFET in subthreshold has a linear/saturation boundary of $V_{DS} \approx 5V_T$, the off-chip voltage reference is an effective way to ensure proper biasing so that the drain voltage is very close to the minimum headroom of M_1 . In the presence of an incoming signal, M_1 is biased at a point where the signal will cause M_1 to pull its drain voltage down far enough to be detected by the comparator, but not too far, so it can do so very quickly.

B. On-chip Voltage Reference and Comparator

An on-chip voltage reference is used in the biasing feedback circuit of the rectifier. Instead of using BJTs, it uses MOSFETs biased in subthreshold which allows for lower power operation as well as enabling the potential for lower supply voltages [6]. The receiver architecture allows for some variance within the voltage reference output so minimal current consumption is prioritized above complete temperature invariance.

A 28nW comparator with programmable hysteresis [7] is used to compare the active and replica outputs from the rectifier and toggle the output of the receiver high or low. The input devices are biased in subthreshold which help the comparator maintain speed while operating at nano-watt power levels. Programmable asymmetric hysteresis is implemented to help offset the impact of mismatch in the rectifier, which will be discussed in the next section.

IV. MISMATCH

Mismatch is significant in the subthreshold region and requires careful design to control. The largest form of mismatch in the receiver comes from the difference between the output of the active and bias rectifiers. The first priority for compensating mismatch in the receiver is through the programmable hysteresis in the comparator. The comparator's programmable hysteresis has a range of +/- 30mV with a resolution of around 2mV. Monte Carlo simulations show this range will satisfy mismatch in over 50% of the chips.

If mismatch is more significant than the range of the comparator and current DACs can handle, then both active and replica rectifiers can be self-biased independent of each other. The rectifier is capable of a second mode of operation where two feedback amplifiers are used, individually sensing the drain voltages of M_1 and M_2 and comparing them against the

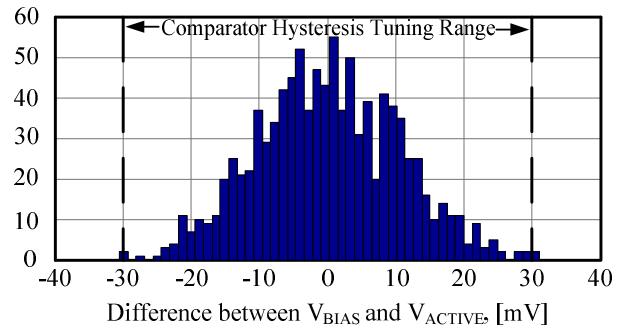


Figure 4. Mismatch between V_{active} and V_{bias}

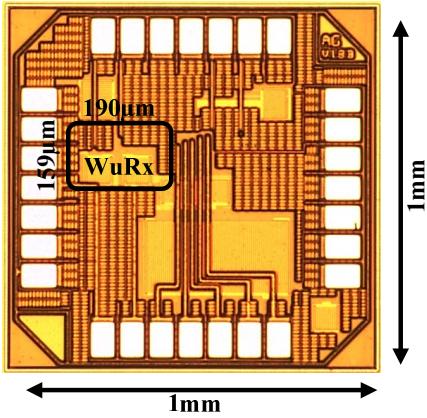


Figure 5. Die Photo

same on-chip voltage reference. Monte Carlo simulations show that the mismatch in this case stays within the +/-30mV range of the hysteretic comparator as shown in Figure 4. The tradeoff with this approach is a reduction in sensitivity due to the feedback amplifier sensing the drain voltage on the active rectifier side.

V. RESULTS

The ultra-low power receiver was fabricated in $0.13\mu\text{m}$ CMOS and operates under a single 1.2V power supply. The active area of the wake up radio is $156 \times 190 \mu\text{m}^2$ and can be seen in Figure 5.

A 100kbps OOK modulated 915MHz signal with -41dBm sensitivity was connected directly to the receiver input and the signal output was monitored on an oscilloscope. Communication using patch antennas was also verified at a distance of 4ft using a transmit power of 0dBm, which is roughly half the theoretical communication distance of 8.5ft based on the Friis equation.

Figure 6 shows the measured output voltage of the rectifier as a function of input signal amplitude. With higher input amplitude, the conversion gain improves which allows

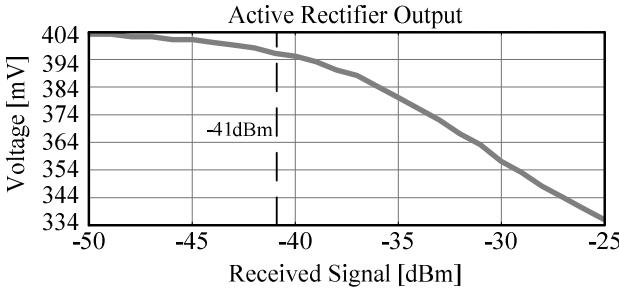


Figure 6. Voltage drop on Active Rectifier

	[2]	[3]	[8]	This Work
Power [μW]	52	51	500	0.098
Sensitivity [dBm]	-72	-75	-37	-41
Frequency [MHz]	2000	915	916.5	915
Data Rate [kbps]	100	100	1000	100
Energy/bit [pJ/bit]	520	510	500	0.98
Die Area [mm^2]	0.1	0.36	1.82	0.03
VDD [V]	0.5	0.5	1.4	1.2
Technology [nm]	90	90	180	130

Table 1: Comparison with State of the Art

for potential power savings. For example, at -30dBm, the power consumption of the receiver can be reduced to 53nW.

Table 1 shows a comparison with other low power radios. It is easy to see the effect RF transconductance has on the power of the other receivers. While the sensitivity in this proposed receiver is reduced compared to [2] and [3], it's very similar to [8].

VI. CONCLUSION

By avoiding the need for RF transconductance and utilizing subthreshold design throughout the circuit, a 98nW receiver was presented. Designed in $0.13\mu\text{m}$ CMOS, the receiver has a sensitivity of -41dBm and a data rate of 100kbps, giving it an energy efficiency of 0.98pJ/bit.

VII. ACKNOWLEDGMENT

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VIII. REFERENCES

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