A LOW-MASS HIGH-SPEED µGC SEPARATION COLUMN WITH BUILT-IN FLUIDIC CHIP-TO-CHIP INTERCONNECTS

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ABSTRACT

This paper reports a low-mass high-speed separation column with built in fluidic chip-to-chip interconnects for a micro gas chromatograph. The 25cm-long suspended column has been successfully coated, and separations have been obtained. The column can be heated to 100°C with 200mW in air and only 80mW in vacuum. The corresponding thermal time constants are 1.2sec and 2.5sec, respectively. Built-in heated interconnects eliminate cold-spots from long and difficult to heat capillary tubes, and plug directly into the preconcentrator and chemi-resistive detector chips, miniaturizing the fluidic analysis path to a size compatible with eventual use in devices such as cellular phones.

INTRODUCTION

Devices for analyzing the chemical composition of gaseous mixtures are badly needed for applications in environmental monitoring, food processing, health care, and homeland security. Gas Chromatography (GC) is well suited to these needs, with the ability to separate volatile organic compounds (VOCs) in an unknown gaseous mixture at sub-ppb detection limits. The gaseous mixture is passed over a preconcentrator where the gases are adsorbed on a bed of carbon. The collected VOCs are then thermally desorbed and passed through a long capillary column, from which they emerge separated in time. A detector (e.g., based on thermal conductivity, chemi-resistive absorption, flame-ionization, or mass spectrometry) converts the separated gases into electrical outlet signals that can be processed and communicated as needed.

Traditionally, GC is carried out in an analysis laboratory using a bench-top instrument that is loaded with gas samples collected in the field. These machines are large, use consumables, require significant amounts of power, and are not portable enough for direct field use. To meet emerging needs, the cycle time between collection and analysis must be dramatically shortened. The best way to do this is to develop MEMS-based wireless µGC systems capable of long-term unattended operation in the field with drastically reduced size, cost, and power, using no consumables, and running on energy scavenged from the environment. The key to realizing these µGC microsystems is the ability to miniaturize the fluidic analysis path (precon/injector, separation column, detector, pump) and use an air carrier. Considerable progress has been reported [1-3] in miniaturizing all of these components, with the ultimate goal of putting the entire microsystem into the volume of a cell phone or wristwatch. A hybrid rather than monolithic [4] realization of the fluidic path is important since the interior of the separation column must be chemically treated while the detector and preconcentrator are not.

Small size reduces power and permits faster analysis using temperature programming. Most µGC columns reported in the past [1-3] have been based on the DRIE etching of rectangular channels in silicon that are capped with an anodically-bonded glass plate. Recently some groups have explored the use of eutectically-bonded silicon capping wafers [5]. Still lower operating power and faster thermal time constants have been achieved with CVD-sealed columns [4,6], eliminating the mass of the glass plate; however, channel walls formed by thin PECVD dielectrics are fragile and difficult to realize with high yield. These systems have also used capillary interconnects between the various components, further increasing system size and producing cold spots that lead to band-broadening and reduced resolution. This paper reports a low-mass column that incorporates chip-to-chip fluidic interconnects, allowing it to plug directly into a preconcentrator and chemiresistive detector to realize a complete µGC analysis system (Fig. 1).

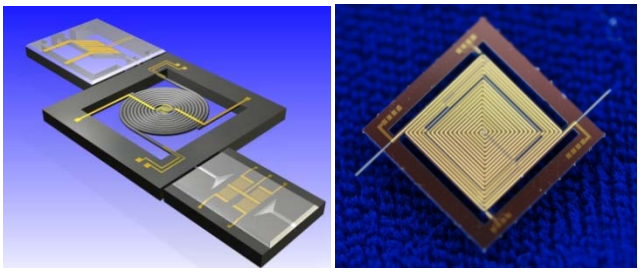

Figure 1: Left: Drawing of complete µGC analysis system. Right: A 25cm-long separation column with built-in fluidic interconnects.

DESIGN CONSIDERATIONS

One of the major challenges in realizing very small, portable GC systems is power. Lower power requires greatly reduced mass and improved thermal isolation. The column reported here is thermally isolated from its surrounding rim, which is maintained at ambient temperature, and has substantially-reduced mass and power requirements compared to previous silicon-glass columns.

In addition to drastically reducing power requirements and increasing speed of operation, the columns must be manufacturable with high yields and must be robust enough for integration in field deployable systems. The column channel structure must provide low mass, an impermeable wall that is strong enough for field use, and a large enough cross-sectional area to enable optimal flow rates for a pump limited to a total pressure drop of about 350Torr.

To minimize the mass and also strengthen the column, a boron-doped silicon layer was added to the previous CVD oxynitride columns [4]. This provides increased strength, accurate thickness control (12µm±1µm), and a very low permeation rate, as compared to 1-2µm thick oxynitride columns, which were previously reported. The design of the column ceiling was also modified using an improved masking structure to achieve greater shape control and yield. Earlier CVD-sealed columns used etch-access patterns (lines [6] or slashes [4]) that were susceptible to stress-induced curl, making sealing difficult. This stress issue was solved using a grid pattern of holes. It was found that 5µm x 5µm holes with 3µm spaces gave the most desirable final column shape. The final etch access pattern was seven holes wide, yielding a ceiling grid width of 53µm.

The design challenges posed by the column coating process, performed after fabrication and prior to final system assembly, are addressed by a combination of strengthened sidewalls and a multiple rim device structure. This coating process requires the stationary phase, dissolved in a solvent, to flow through the column and then for the column to be sealed and a vacuum pulled to evaporate the solvent [7]. Traditionally, we have attached capillary tubes to the column for the coating and then used the same capillaries for interconnects in the final system. Since this system has integrated interconnects, the capillary tubes are designed to be removed once the coating and characterization process is complete. A sacrificial inlet and outlet structure was designed which provides connection ports for the capillary tubes and mechanically isolates them from the column using a secondary support rim. After the column is coated and tested, it is laser cut out of the sacrificial outer rim (Fig. 2), leaving only the final inlet and outlet tubes (Fig. 3) and a narrow inner rim that provides structural support, thermal isolation, and bond locations for the heaters and temperature sensors

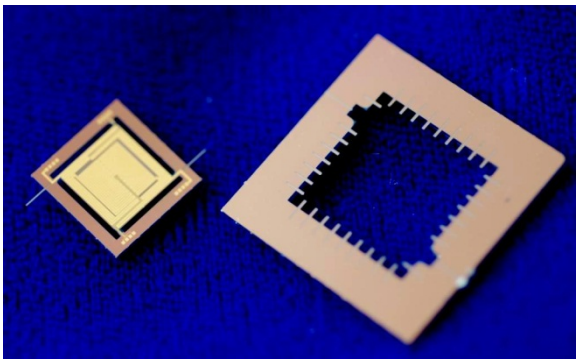

Figure 2: Column cut out of the sacrificial rim after coating, leaving pristine inlets and outlets to connect to the final system.

COLUMN FABRICATION

Fabrication begins with the deposition of a 1µm dielectric film that has a stress of about 200MPa tensile designed to offset the stress of the deep boron diffusion. We deposit a stack of High Temperature Oxide (HTO), silicon nitride, and HTO that has a 2.2:1 ratio or for a 1µm-thick stack (310/300/340nm) with a stress of 210MPa. The HTO is deposited at 910°C and the Si_3N_4 at 810°C.

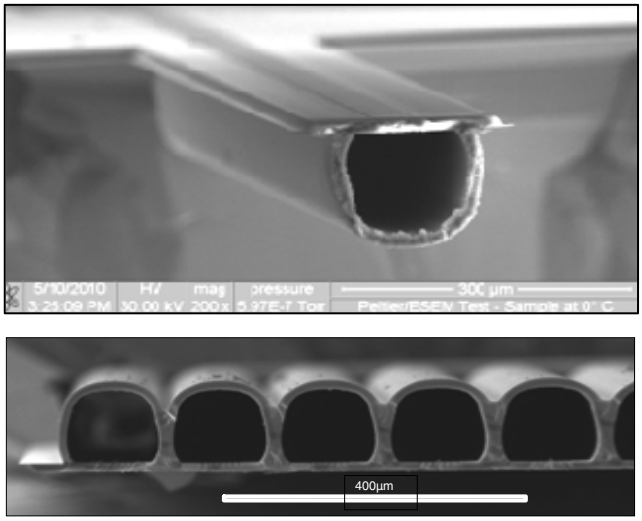

Figure 3: Cross-sections of the laser-cut fluidic interconnects and the column cross-section. The flow channel is 120µm across and 90µm deep.

The backside dielectrics are then pattered. This is followed by etching holes in the top dielectric to allow access to the silicon for column formation. As mentioned previously, a grid pattern was chosen for this because of its mechanical stability. With the stress change induced by the deep boron diffusion, this was a significant concern. A grid of holes will stay intact and remain planar under a wide range of film stress conditions, allowing the devices to be sealed. Careful stress management is important (Fig. 4).

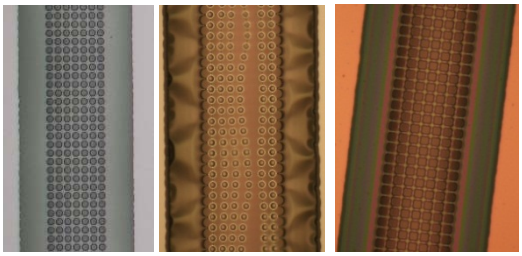

Figure 4: Left: low-stress dielectric ceiling after column etch and before boron diffusion. Center: a wafer that started with a low-stress film before etching and boron diffusion. Right: a wafer that started with a 210MPa tensile dielectric film before etching and boron diffusion

After the dielectric layer is patterned, the photoresist is left in place and the wafer is etched in an STS Deep Silicon Etcher. Initial etching is done using a standard anisotropic deep silicon dry etch followed by an isotropic dry silicon etch. Etch details are given in Tables 1 and 2. The final cross sections can be seen in Fig. 3.

The photoresist is then striped using and the wafers are cleaned using the standard RCA process before deep boron diffusion. The first step is 5 hours at 1175°C with solid

boron disks as the boron sources. The wafers are then transferred to a drive in furnace for another 5 hours at 1175°C. The channels are now formed and the walls are boron diffused. Next the grid at the top is sealed using 12µm of PECVD oxynitride. The top film needs to have very low stress and in this case is 2.7MPa tensile.

Table 1: Anisotropic Si Etch

Etch		*Passivation*	
Time (sec)	13	Time (sec)	7
SF6 Flow (sccm)	160	SF6 Flow (sccm)	0
CF4 Flow(sccm)	0	CF4 Flow(sccm)	85
Coil Power (W)	800	Coil Power (W)	600
Platen Power (W)	250	Platen Power (W)	0

Table 2: Isotropic Si etch in STS

SF6 Flow (sccm)	260
CF4 Flow (sccm)	0
Ar Flow (sccm)	5
Aperture (5)	50
Coil Power (W)	800
Platen Power (W)	60

Once the column has been sealed, heaters and temperature sensors can be deposited. A 20/30/200nm stack of Ti/Pt/Au is deposited using liftoff. To complete the front side processing, the dielectric layer is patterned. SPR220 3.0 is used as a mask. The 12µm of oxynitride and top 340nm of SiO_2 are etched for 32 minutes in buffered HF using a two-step etching process. The remaining dielectric is removed using dry etching. Finally, the front side of the silicon is recessed 40µm using DRIE. Removal of the photoresist concludes the front-side processing for these devices.

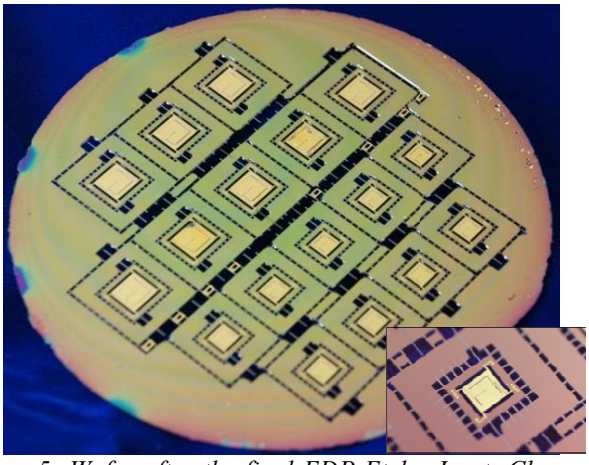

Figure 5: Wafer after the final EDP Etch. Inset: Close-up of CVD-sealed 25cm µcolumn.

Processing resumes on the backside with a 6µm layer of photoresist that is patterned and used as an etch mask for DRIE. Before the wafer is etched it is mounted on a carrier wafer. The wafer is etched until the deepest spot is 300µm from the backside of the wafer. The photoresist is removed, and the device wafer separated from the carrier wafer. Finally, the wafer is immersed in an ethylenediamine pyrocatechol (EDP) bath at 110°C until the columns and inlet/outlet connections are etched clear. The column rim is now held in an outer rim (Fig. 5) by silicon support tabs so that the double-rim structure is still part of the intact wafer. The die can be separated with a diamond scribe. The ends of the column are opened using laser cutting.

TESTING

Separations

A special jig (Fig. 6) is used to hold the device during the coating and characterization steps. The opening in the jig aligns the column ports to grooves which guide the capillary tubes during connection and provide strain relief. After a column is positioned and taped down, epoxy is applied to a port, the capillary tube is slid into place and mechanically stabilized with a piece of tape. The process is repeated for the other port.

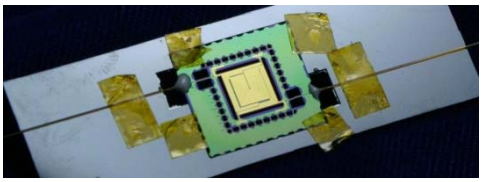

Figure 6: A CVD sealed column in a coating jig with capillaries attached.

Columns were successfully coated using the static column coating technique [7] to give a 100nm-thick stationary phase of polymethylsiloxane. A five-component alkane mixture (Fig. 7) was then introduced and isothermally separated. An Agilent 7890 GC sample injection and FID was used.

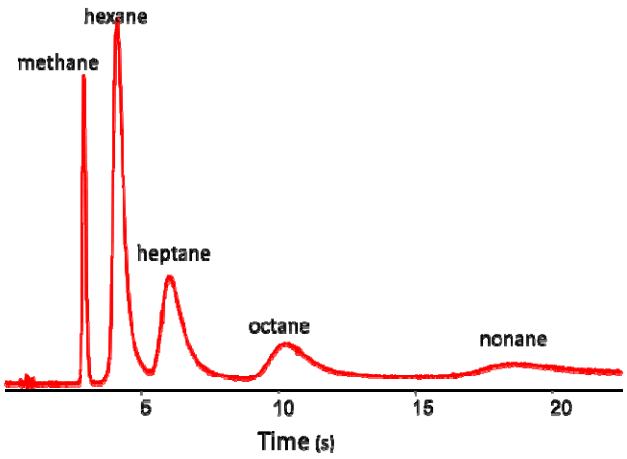

Figure 7: Chromatogram of a gas alkane mixture measured using a 25cm-long CVD-sealed microcolumn.

Heating and Cooling

The columns were heated with the on-column heaters to 100°C in both air and in a vacuum. In air, it required 200mW at 6.3V and 31.75mA to reach 100°C; in vacuum it

required 78mW at 3.95V and 20mA. The measured thermal time constants are 1.2sec and 2.5sec as shown in Fig. 8.

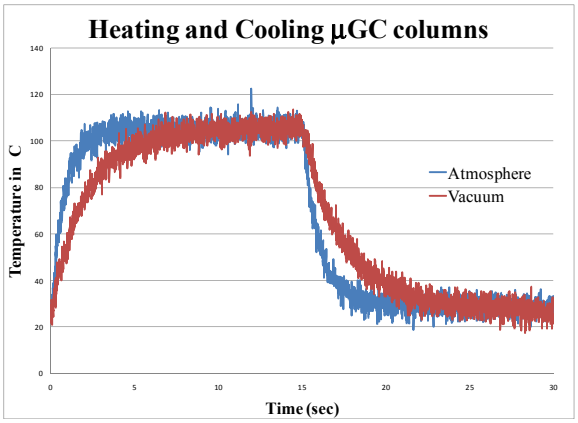

Figure 8: Heating from a 25°C ambient to 100°C and then cooling to 25°C for a 25cm CVD-sealed microcolumn.

FINAL ASSEMBLY

The assembly and mounting of the fluidic analysis path is accomplished with a micromachined silicon frame (Fig. 9) which serves as the mechanical package, alignment/assembly jig and electrical interconnect. The separation column is positioned and secured in the center cavity with the inlet and outlet tubes extending out towards the mating devices. The preconcentrator and detectors are placed at the outboard ends of the slide regions which provide lateral and vertical alignment between their ports and the tubes on the column. The devices slide together and an adhesive sealant is applied to make a leak-free connection. Once assembled all the components are secured to the jig with adhesive and wirebonds are made between the device pads and the interconnection pads on the jig. Capillary tube connections to the preconcentrator and detector are made and the tubes are restrained at the outboard ends of the jig (not shown).

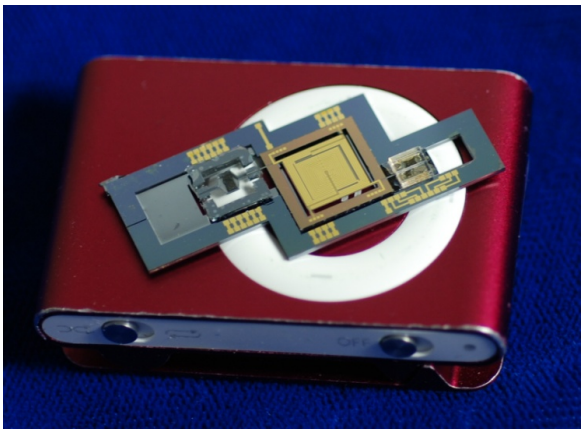

Figure 9: A 25cm separation column, single-bed preconcentrator, and chemi-resistive detector on a 2nd generation Apple iPod Shuffle about the size of the intended µGC system. The outer circle is about the size of a U.S. quarter.

CONCLUSIONS

A low-mass high-speed column for a micro gas chromatograph has been fabricated and coated. Separations have been performed using this column, and the thermal response has been tested. Capillary attachments for column coating and their subsequent removal are provided using a sacrificial double-rim structure. Assembly of the fluidic path is facilitated using a custom-designed silicon platform.

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