THIN-FILM TRANSISTORS

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MARCEL DEKKER, INC. NEW YORK • BASEL

Library of Congress Cataloging-in-Publication Data
A catalog record for this book is available from the Library of Congress.

ISBN: 0–8247–0959–4

This book is printed on acid-free paper.

Headquarters
Marcel Dekker, Inc.
270 Madison Avenue, New York, NY 10016
tel: 212–696–9000; fax: 212–685–4540

Eastern Hemisphere Distribution
Marcel Dekker AG
Hutgasse 4, Postfach 812, CH-4001 Basel, Switzerland
tel: 41–61–260–6300; fax: 41–61–260–6333

World Wide Web
http://www.dekker.com

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Current printing (last digit):
10 9 8 7 6 5 4 3 2 1

PRINTED IN THE UNITED STATES OF AMERICA

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3

Hydrogenated Amorphous Silicon Thin-Film Transistors

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3.1 MOTIVATION

This chapter focuses on issues related to the engineering of high-performance hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) suitable for large-area high-resolution active-matrix liquid crystal displays (AMLCDs). In particular, the underlying physics, numerical simulation, and characterization of a-Si:H TFTs and a-Si:H advanced TFT structures are described.

Ever since the solid-state revolution, silicon-based devices and integrated circuits have replaced most of the conventional circuitry in electronics. The change is so significant that the lives of almost everyone in the world have been affected. Vacuum tubes, once dominant composing elements of electronic appliances such as computers and radios are now historic exhibits and can hardly be seen without going to a museum. However, vacuum tubes have not completely disappeared from our lives. The giant vacuum cathode ray tubes (CRTs) still remain the major information display terminal for television and computers. Yet

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the CRT is gradually being replaced by the emerging technology of flat-panel displays (FPDs). The advantages of FPDs are obvious, especially for portable applications such as laptop computers, medical imaging X-ray sensors, and avionic displays. Today, it is also clear that the heavy and bulky CRTs will soon become history just like their other vacuum counterparts. In fact, the commerical battle between CRTs and FPDs is very intense. The main reason for FPDs' not having completely taken over the CRT market is that they cost more than CRTs, but the gap is closing every year. In fact, 2003 is expected to be the first year when FPD revenue will exceed that of CRTs.

Among various FPDs, the dominant product on the market is liquid crystal displays (LCDs). There are two types of LCDs: passive and active addressing modes; the advantages of the former lay in its low cost, while the latter enables high-resolution displays. For active-matrix LCDs, silicon (amorphous or polycrystalline) thin-film transistors serve as the key pixel electrode–switching element. Hydrogenated amorphous silicon is well suited for AMLCDs because it can easily be deposited over large areas at low temperatures that are fully compatible with glass or plastic substrates. In addition, it has a high dark resistivity, leading to TFTs with low leakage currents. Films of a-Si:H can be *n*- or *p*-doped to allow for the fabrication of low-resistance contacts. The processing of a-Si:H TFTs is similar to the crystalline silicon metal oxide–semiconductor (MOS) integrated circuit technology, which makes AMLCDs more mature than other technologies, such as organic displays based on light-emitting devices. Finally, a-Si:H technology benefits from the tremendous investment in a-Si:H solar cells made several years ago, and so has become the dominant player in the active-matrix display world.

3.2 NUMERICAL SIMULATION OF AMORPHOUS SILICON THIN-FILM TRANSISTORS

Since hydrogenated amorphous silicon thin-film transistors were described by LeComber et al. in 1979 [1], they have been widely used as switching devices in active-matrix liquid crystal displays [2]. To improve the electrical performance of a-Si:H TFT for high-resolution AMLCDs, for instance, it was important to evaluate how the a-Si:H density-of-states (DOS) and the TFT source/drain series resistances affect the device electrical performance [3–5]. It was expected that a good understanding of a-Si:H physics combined with the a-Si:H DOS model would substantially reduce the time and cost of a-Si:H TFT process optimization.

Device modeling can be preliminarily divided into two fields: analytical modeling and numerical modeling. In the early days only analytical modeling could be achieved because of limited computer resources for numerical modeling. The advantage of analytical modeling of a-Si:H TFTs [6–9] is that the device performance and design parameters are related by a closed-form equation, helping

the understanding and improvement of the device electrical performance. Furthermore, analytical modeling can be integrated easily into existing CAD tools such as SPICE for circuit simulation. However, for a device with more complicated materials or structures, it is difficult to derive a closed-form equation that can represent the device physics. For instance, it is more difficult to model a-Si:H TFTs analytically than metal oxide–silicon field-effect transistors (MOSFETs) because the a-Si:H large density-of-states makes it difficult to solve Poisson's equation and other differential equations. Furthermore, analytical modeling has difficulty dealing with two- or higher-dimensional structures. Therefore, analytical modeling often has to simplify the device structure into one dimension. However, some structures, such as the a-Si:H TFT with thin semiconductor layer, cannot be simplified into a one-dimensional structure, and any simplifying assumptions made during the derivation will limit the accuracy of obtained results.

Although it is time consuming and difficult to incorporate into circuit simulators, numerical modeling usually provides a more flexible method in the modeling of devices, so different model assumptions may be analyzed and compared. The numerical method resolves basic semiconductor equations such as Poisson's and continuity equations without any simplifications. Based on these equations, the influence of different distributions of density of states and source/drain contact resistances can be analyzed from the point of view of two-dimensional current flow.

3.2.1 Simulation Model

Today the most popular structure for a-Si:H TFTs is the inverted-staggered structure shown in Figure 3.1. The semiconductor layer consists of intrinsic a-Si:H and heavily P-doped (n^+) a-Si:H. The gate insulator is usually hydrogenated

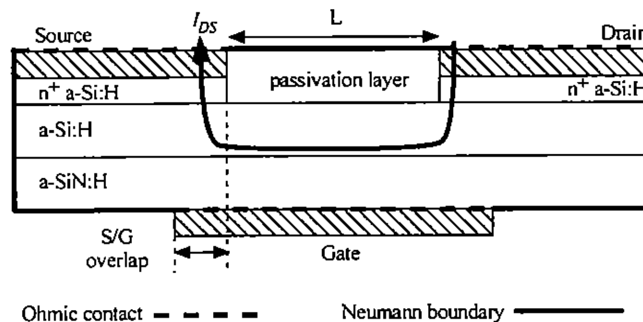

Figure 3.1 Cross section of the a-Si:H TFT structure used for numerical simulations. (Adapted from Ref. 19 with permission from Elsevier Science.)

amorphous silicon nitride (a-SiN_x:H). The inverted-staggered a-Si:H TFT operates in the accumulation mode. When a positive voltage is applied to the gate electrode, the band bending at or near the gate insulator/amorphous semiconductor interface is increased and electrons accumulate near the interface to form the conduction channel. If a positive drain voltage is applied to the drain electrode, the drain–source current flows from the drain to the source electrodes through n^+ a-Si:H, intrinsic a-Si:H, and conduction channel (see Fig. 3.1).

If the electrostatic potential and quasi-Fermi levels are known as a function of position, all the physical phenomena can be determined. To calculate these three variables, the two-dimensional Poisson's equation and continuity equations are solved simultaneously [10]. Poisson's equation is given by

$$\nabla\cdot(\varepsilon\nabla\psi) = q[p - n - \sum(N_A^- - N_D^+)] \tag{3.1}$$

where ε is the permittivity of a-Si:H, ψ is the electrostatic potential, q is the electronic charge, p and n are electron and hole concentrations, respectively, and N_A^- and N_D^+ are the concentrations of ionized acceptor-like and donor-like states, respectively.

The continuity equations for electrons and holes, respectively, are as follows:

$$-\frac{1}{q}\nabla\cdot J_n = G_n - R_n \tag{3.2}$$

$$\frac{1}{q}\nabla\cdot J_p = G_p - R_p \tag{3.3}$$

where J_n and J_p are the current density for electrons and holes, respectively, G_n and G_p are the generation rates ($cm^{-3}s^{-1}$) for electrons and holes, respectively, and R_n and R_p are the recombination rates ($cm^{-3}s^{-1}$) for electrons and holes, respectively. The net recombination rate through every defect state is given by the Shockley–Read–Hall formulation [11].

The two-dimensional a-Si:H TFT structure is decomposed into a discrete mesh structure by the finite-element method. Grid points are placed nonuniformly and depend on the estimated distribution of carrier concentrations. The area near the a-Si:H/a-SiN_x:H interface and the source/drain-gate overlap have denser grid points. A larger number of grid points can improve the accuracy of simulation but will also increase computation time. To ensure an acceptable compromise, the number of grid points is increased until the simulation results are within 2% of variations: for a 10 μm-channel-length a-Si:H TFT, the total number of grid points in our device structure is about 800. Once the grid points are determined and drain and gate voltages are set, the simulation program resolves the nonlinear partial differential equations (Poisson's equation, electron and hole continuity equations) using Newton's method [10] and ψ, n, and p as unknowns. All the physical parameters, such as current, electrostatic potential, electron concentra-

tion, hole concentration, electrical field, and energy band bending, can be calculated.

3.2.1.1 Boundary Conditions

Two types of boundary conditions are used in this simulation: ohmic contact and Neumann (reflective) boundary. These boundaries are illustrated in Figure 3.1. The contacts between source/drain metal and n^+ a-Si:H, and gate metal and gate insulator interfaces are assumed to be ohmic. On the other hand, the outer edges of a-Si:H TFT are assigned to be Neumann boundaries. Ohmic contacts are considered as simple Dirichlet boundaries, where the boundary fixes the electrostatic potential and the electron and hole concentrations along the boundary. For a given specific contact resistance (R_c in Ω-cm^2), the electrostatic potential ψ is determined by

$$\psi = \psi_{\text{ref}} + V_a - \frac{R_c}{A} I_a \tag{3.4}$$

where A is the area of the boundary, $\psi_{\text{ref}} = E_c - E_F/q$ at the terminal, E_F is the Fermi-level position, V_a is the terminal voltage, and I_a is the terminal current.

On the other hand, the outer edges of the a-Si:H TFT are assumed to be limited by the Neumann boundary conditions, so the current flows out of the device only through the drain and source contacts. Assuming no surface charges on such edge, the normal components of the electrostatic potential and carrier concentration gradients are set to zero:

$$\frac{\partial \psi}{\partial \hat{r}} = \frac{\partial n}{\partial \hat{r}} = \frac{\partial p}{\partial \hat{r}} = 0 \tag{3.5}$$

where $\hat{r}$ is the direction perpendicular to the external boundary.

Traditionally, the MOSFET boundary conditions are based on the semi-infinite semiconductor assumption; i.e., the width of the space-charge regions (or the effective Debye length) is much smaller than the thickness of the semiconductor, and the band bending decreases to zero in the bulk of the semiconductor layer ($d\psi/dy = 0$ and $\psi = 0$ at $y = t_{\text{a-Si:H}}$) However, these boundary conditions are not always applicable to a-Si:H thin-film transistors [12–14]. Thin a-Si:H layers (500–2500 Å) and low free-carrier density will allow the depletion region to extend over the entire semiconductor layer. Thus the traditional boundary conditions at the interface between the a-Si:H and the passivation layer cannot be applied to a-Si:H TFTs.

The set of the three-coupled nonlinear partial differential Eqs. (3.1), (3.2). and (3.3) are numerically solved for every grid point at given drain, source, and gate biases. Examples of the simulated static transfer characteristic in linear and

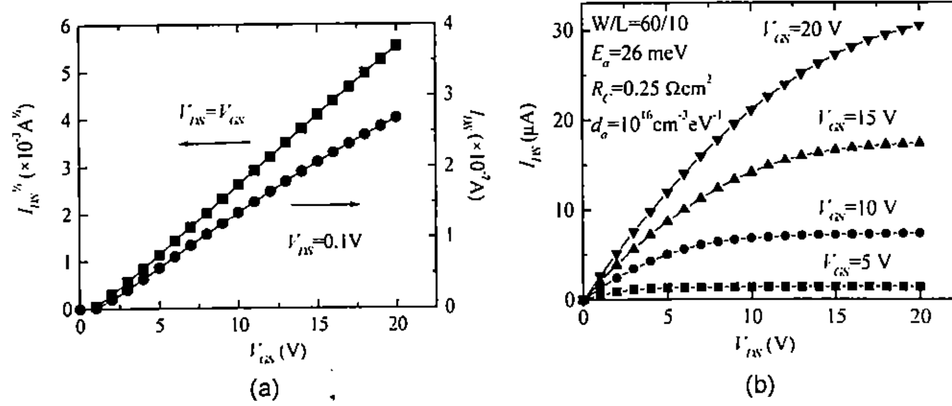

Figure 3.2 (a) Simulated transfer characteristics in linear and saturation regimes. (b) Simulated output characteristics. (From Ref. 15.)

saturation regimes are shown in Figure 3.2a [15]. The field-effect mobility (μ_{FE}) and threshold voltage (V_T) were extracted in linear and saturation regions [16] using the gradual channel approximation equations:

$$I_{DS} = \frac{\mu_{FE}C_iW}{L}(V_{GS} - V_T)\,V_{DS} \tag{3.6}$$

for $V_{DS} = 0.1$ V (linear region), and

$$I_{DS} = \frac{\mu_{FE}C_iW}{2L}(V_{GS} - V_T)^2 \tag{3.7}$$

for $V_{DS} = V_{GS}$ (saturation region), where C_i is the gate insulator capacitance per unit area, L is the channel length, W is the channel width, V_{GS} is the gate–source voltage, and V_{DS} is the drain–source voltage. An example of output characteristics is shown in Figure 3.2b.

3.2.1.2 Amorphous Silicon Density-of-States Model

The model of the density-of-states for a-Si:H proposed by Davis and Mott [17] is adopted in this simulation. The states present in the a-Si:H electronic gap consist of two types: band-tail states and deep-gap states. For numerical simulation, the continuous distributions of both acceptor- and donor-like states within the mobility gap was approximated by several discrete energy states. A total number of

90 discrete energy states with an 0.02 eV interval constitutes a trade-off between accuracy and computation time.

The distributions of band-tail states are given by Eqs. (3.8) and (3.9):

$$g_{CBa} = g_{ta} \exp\left(\frac{E - E_c}{E_a}\right) \tag{3.8}$$

$$g_{VBd} = g_{td} \exp\left(-\frac{E - E_v}{E_d}\right) \tag{3.9}$$

where g_{ta} and g_{td} are the densities of acceptor- and donor-like tail states at $E = E_C$ and $E = E_V$, respectively, and E_a and E_d are the characteristic slopes of the conduction- and valence-band tails, respectively. The valence-band-tail states are below the Fermi level and have negligible influence on a-Si:H TFT electrical characteristics in the ON-state. This is not the case for the conduction-band-tail states, which can significantly affect the a-Si:H TFT electrical performance. Transfer characteristics in the saturation region calculated for different E_a values are shown in Figure 3.3a: the corresponding μ_{FE} decreases and V_T increases when E_a increases. We should note that the lower E_a values are associated with a-Si:H film having an enhanced short-range order.

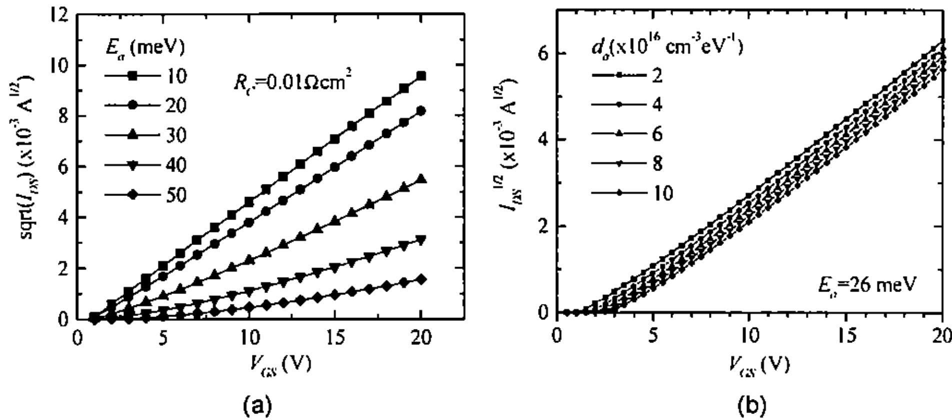

FIGURE 3.3 Simulated transfer characteristics in the saturation regime for (a) different conduction-band-tail slopes and (b) different peak values of deep-gap states. (From Ref. 15.)

The deep-gap states are modeled by two Gaussian-like distributions representing the donor- and acceptor-like traps:

$$g_{DGa} = d_a \exp\left(-\frac{(E - \lambda_a)^2}{\sigma_a^2}\right) \tag{3.10}$$

$$g_{DGd} = d_d \exp\left(-\frac{(E - \lambda_d)^2}{\sigma_d^2}\right) \tag{3.11}$$

where d_a and d_d are the peak values of the Gaussian distribution of acceptor- and donor-like deep-gap states, respectively, λ_a and λ_d are the mean energies of the Gaussian distributions of acceptor- and donor-like states, respectively, and σ_a and σ_d are the standard deviations of the Gaussian distributions of acceptor- and donor-like states, respectively. The description and default values for these equations and typical geometry parameters used in this simulation are listed in Table 3.1.

Simulated transfer characteristics are plotted in Figure 3.3b for peak values of deep-gap states, d_a ranging from 2×10^{16} to 10^{17} $cm^{-3}eV^{-1}$. The TFT field-effect mobility is not affected, but the threshold voltage increases with increasing d_a.

3.2.1.3 Source and Drain Contact Resistances

Based on the current flow shown in Figure 3.1, the a-Si:H TFT source/drain series resistances consist of three parts: (1) the specific contact resistances between the source/drain metal electrodes and the n^+ a-Si:H layers; (2) the resistances of n^+ a-Si:H film; and (3) the resistances due to the intrinsic a-Si:H layers between the source/drain n^+ a-Si:H layers and the conducting channel (a-Si:H/a-SiN_x:H interface). Parts (2) and (3) will be discussed in section 3.3.4.

In general, the contact resistance depends on the specific contact resistance (R_C) and the contact area. Today R_C is limited by the poor doping efficiency of n^+ a-Si:H, and it is about 0.1–1 Ω-cm^2 with current a-Si:H TFT technology. For a given source/drain metallurgy, one way to reduce the contact resistance is to increase the doping efficiency of n^+ a-Si:H. Kanicki [18] showed that when the n^+ a-Si:H film resistivity (R_f) is reduced from 100 to 10 Ω-cm, the R_C decreases from 30 to 0.1 Ω-cm^2. The experimental relation between R_f (in Ω-cm) and R_C (in Ω-cm^2) for Mo/n^+ a-Si:H contacts can be described by [18]

$$\log(R_c) = -1 + 1.25 \log(R_f) \tag{3.12}$$

For large R_C, a nonnegligible portion of the applied drain voltage drops on the high source/drain contact resistances, leading to a reduced field-effect mobility [19].

TABLE 3.1 Parameters Used for the Numerical Simulations, Unless Specified Otherwise

Parameter	Value	Description
λ_a (eV)	0.98	Mean value of Gaussian-distributed acceptor-like deep-gap states
σ_a (eV)	0.2	Variance of the Gaussian-distributed acceptor-like deep-gap states
λ_d (eV)	0.56	Mean value of the Gaussian-distributed donor-like deep-gap states
σ_d (eV)	0.17	Variance of the Gaussian-distributed donor-like deep-gap states
σ_n (cm^2)	10^{14}	Electron capture cross section of the conduction-band-tail states
μ_{n0} (cm^2/Vs)	8	Electron mobility in conduction-band extended states
σ_p (cm^2)	10^{14}	Hole capture cross section of the valence-band-tail states
μ_{p0} (cm^2/Vs)	6	Hole mobility in valence-band extended states
ε_{SiN}	6.9	Dielectric constant of the gate insulator
d_a ($cm^{-3}eV^{-1}$)	10^{16}	Peak value of Gaussian-distributed acceptor-like deep-gap states
d_d ($cm^{-3}eV^{-1}$)	10^{16}	Peak value of Gaussian-distributed donor-like deep-gap states
E_a (meV)	26	Conduction-band-tail characteristic energy
E_d (meV)	55	Valence-band-tail characteristic energy
E_G (eV)	1.8	Band gap of a-Si:H
g_a ($cm^{-3}eV^{-1}$)	10^{21}	Density of states at E_c
g_d ($cm^{-3}eV^{-1}$)	10^{21}	Density of states at E_v
L (μm)	10	Channel length
d (μm)	3	Source/drain gate overlap
R_c (Ωcm^2)	0.25	Source/drain specific contact resistances
R_t (Ωcm)	1.25	n^+ a-Si:H film resistivity
$t_{a\text{-}Si:H}$ (μm)	0.25	a-Si:H film thickness
t_{nSi} (μm)	0.07	n^+ a-Si:H film thickness
$t_{a\text{-}Si:N}$ (μm)	0.35	a-SiN_x:H (gate insulator) film thickness
W (μm)	60	Channel width

3.2.2 Temperature Effect on Amorphous Silicon Thin-Film Transistors

Transfer characteristics simulated at different temperatures ranging from 300 to 420 K at $V_{DS} = 0.1$ V show temperature-activated behavior, and the field-effect activation energy E_{act} can be calculated from the Arrhenius plot, i.e., the slope of $\log(I_{DS})$ versus $1/T$ plot at a given V_{GS}.

An increase in the density of the deep-gap states causes only a threshold voltage shift and consequently no change of the $E_{act} - V_{GS}$ curve above threshold [20]. On the other hand, the conduction-band-tail has a significant effect on the activation energy curve. Figure 3.4 shows the $E_{act} - V_{GS}$ curves calculated for various conduction-band-tail slopes. The field-effect activation energy clearly increases with increasing density of conduction-band-tail states. An increase of the energy difference between the conduction-band edge and the Fermi level (at 0 K) can also be observed [21].

An experimental result is also given in Figure 3.4: Simulation cannot explain the experimental curve. This can be achieved by considering the temperature dependence of the source/drain series resistance. By adding temperature activated behavior of the S/D contact resistances and resistances of the n^+ a-Si:H layers, good fit can be obtained between the experimental and simulated field-effect activation energy curves [21].

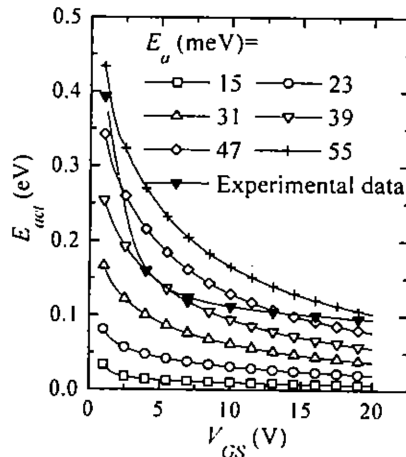

FIGURE 3.4 Simulated evolution of the a-Si:H TFT field-effect activation energy for various conduction-band-tail slopes. (From Ref. 15.)

3.2.3 Amorphous Silicon Thin-Film Transistors Under Illumination

The numerical simulation program developed for the analysis of the a-Si:H TFT under illumination [22,23] is similar to the one described earlier, used in the dark. It solves simultaneously the three equations describing the steady-state conduction in semiconductors: the Poisson equation, electron and hole continuity equations, out of thermal equilibrium, using the Shockley–Read model for the carrier recombination rate. The amorphous silicon density-of-states is modeled by two exponential band tails and two Gaussian distributions of monovalent states, where the recombination process takes place. The program takes into account the a-Si:H density-of-states at the interfaces (a-Si:H/a-SiN_x:H and back-channel interfaces) and in the bulk of the semiconductor. The gate insulator is assumed to be ideal; i.e., there is no charge trapping or fixed charge present in the insulator layer. The TFT is illuminated from the source–drain side, and we assume that the whole a-Si:H layer is exposed to the light. The spatial resolution of the three-equation set is achieved over the whole a-Si:H TFT structure by defining an irregular 2D mesh, thinner at the interfaces between two different layers. For each set of input conditions (voltages and illumination conditions), we obtain, at every node of the 2D mesh, the values of the three unknowns: electrostatic potential and electron and hole Fermi potentials. These values allow us to deduce 2D maps of the physical parameters, such as the current densities, carrier densities, and electric field.

Figure 3.5 shows the TFT transfer characteristics simulated in the dark and under a uniform monochromatic illumination. We can distinguish both the a-Si:H TFT electron and hole threshold voltages, which delimit three main TFT operating regimes [24]:

(I) electron accumulation layer created at the a-Si:H/a-SiN_x:H interface;
(II) no accumulation layer;
(III) hole accumulation layer created at the a-Si:H/a-SiN_x:H interface.

In regime (I), the TFT drain current is associated with the drift diffusion of electrons in the accumulation layer (conduction channel). In regime (II), the TFT drain current results from the same mechanism as in regime (I), but the conduction occurs uniformly in the whole amorphous silicon layer (channel and bulk), since there is no carrier accumulation at the a-Si:H/a-SiN_x:H interface. Because the carrier densities in the whole amorphous silicon layer depend mostly on the light-induced generation and carriers recombination rates, in this regime the TFT drain current is sensitive to the amorphous silicon thickness and to the bulk density of states of amorphous silicon. In regime (III), the existence of the hole accumulation layer at the a-Si:H/a-SiN_x:H interface, in combination with

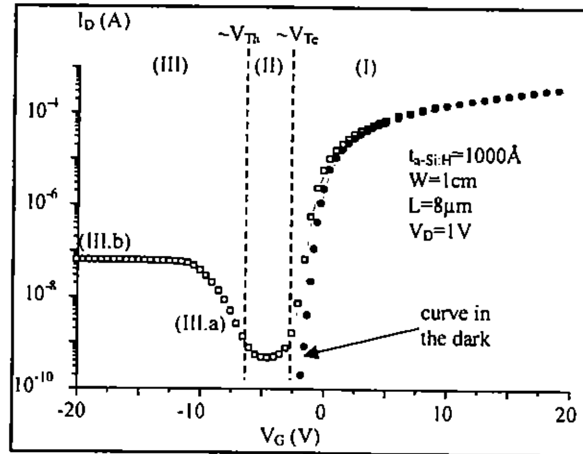

Figure 3.5 Simulated a-Si:H TFT transfer characteristics under illumination and in the dark. (From Ref. 23, with permission from Society for Information Display.)

the $n+$ a-Si:H source/drain contact layers, results in a situation similar to two a-Si:H *pn* junctions located at the source and drain access areas. For a positive drain voltage, the source and drain junctions are, respectively, in the ON- and OFF-state.

We can actually distinguish two different conduction regimes within regime (III): In regime (III.a), the TFT current increases with the magnitude of the gate voltage, while it reaches a plateau in (III.b). The distinction between these two regimes depends on the relative importance of two different physical mechanisms: In regime (III.a), the drift diffusion of holes in the accumulation layer (conduction channel) is predominant, whereas in regime (III.b) the recombination of electrons and holes in the drain (OFF-state) *pn* junction depletion region is the most important. We should note that the importance of the source junction has been mentioned in [25], but we do not think that it is critical in regimes (III.a) and (III.b). Figure 3.6 shows the simulated variations of the electron and hole Fermi potentials along the usual TFT current path between the source and drain contacts. We can see that, in regime (III.a) (here for $V_G = -7.5$ V), the main variation of the Fermi potentials happens in the accumulation layer, where the drift diffusion of holes occurs. The conduction in this regime is similar to the conduction when the TFT is in the accumulation regime (gate voltage larger than the electron threshold voltage); however, in this regime the majority carriers are the holes

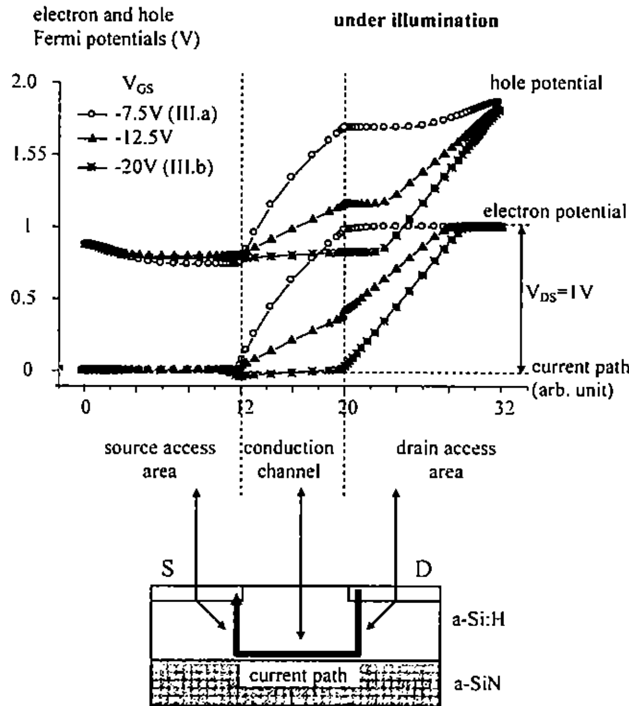

FIGURE 3.6 Simulated variations of the electron and hole Fermi potentials along the main TFT current path under illumination. (From Ref. 24.)

instead of the electrons. In contrast, in regime (III.b) (here for $V_G = -20$ V), the main variation of the Fermi potentials occurs in the drain *pn* junction depletion region, where the recombination of electrons and holes is taking place. Photogenerated current at the drain junction is the lowest [25] and is therefore the bottleneck in the process. Consequently, the a-Si:H TFT current depends only on the light-induced generation and recombination of electrons and holes in the drain *pn* junction depletion region. Actually, for high negative voltages, the recombination rate can be neglected, and the TFT current is therefore set only by the light-induced generation of electrons and holes (as in a photodiode case). This can explain why, in this regime, there is no longer any influence of the gate voltage (saturation phenomenon) or channel length on the TFT drain current as observed experimentally [23]. However, we should note that this saturation regime is not always reached for typical values of the gate voltage.

The parameters that influence the a-Si:H TFT drain current depend on the TFT operation regime to be considered. The electron and hole threshold voltages depend mostly on the amorphous silicon density-of-states associated with both the a-Si:H/a-SiN_x:H interface and the bulk a-Si:H; the difference between the two threshold voltages is higher for a larger density-of-states. In regime (II), the TFT drain current depends strongly on the amorphous silicon thickness but also on the a-Si:H bulk density-of-states; it increases with a-Si:H thickness and decreases with a-Si:H density-of-states. The drain current in regime (III.b) depends only on the light-induced generation of electron–hole pairs in the drain *pn* junction depletion region (between the drain contact and the a-Si:H/a-SiN_x:H interface); it increases with the illumination intensity and with the *pn* junction area.

3.3 AMORPHOUS SILICON THIN-FILM TRANSISTOR CHARACTERIZATION

3.3.1 Normalization of Thin-Film Transistor Characteristics

a-Si:H TFT transfer characteristics need to be normalized to accurately compare samples with different geometric parameters and/or different gate insulators [26]. First, in order to take into account the geometrical dependence of the TFT characteristics in the linear regime, we should use the normalized TFT conductance (in Ω^{-1}) instead of the TFT drain current:

$$G = \frac{I_{DS}}{V_{DS} W/L} \tag{3.13}$$

where V_{DS} is the source–drain voltage and W and L are the TFT channel width and length, respectively.

Then instead of the gate voltage, we should use the electrical charge induced by the gate voltage at the amorphous semiconductor/gate insulator interface (in C/cm^2):

$$Q_{\text{ind}} = V_{GS} \times C_i \tag{3.14}$$

where C_i is the insulator capacitance per unit area. Alternatively, we can use G/Ci versus V_{GS} characteristics for the analysis of the TFT linear regime.

In the TFT saturation regime, we should use the normalized TFT current expressed by

$$I_{DS\text{norm}} = \frac{I_{DS}}{C_i W/2L} \tag{3.15}$$

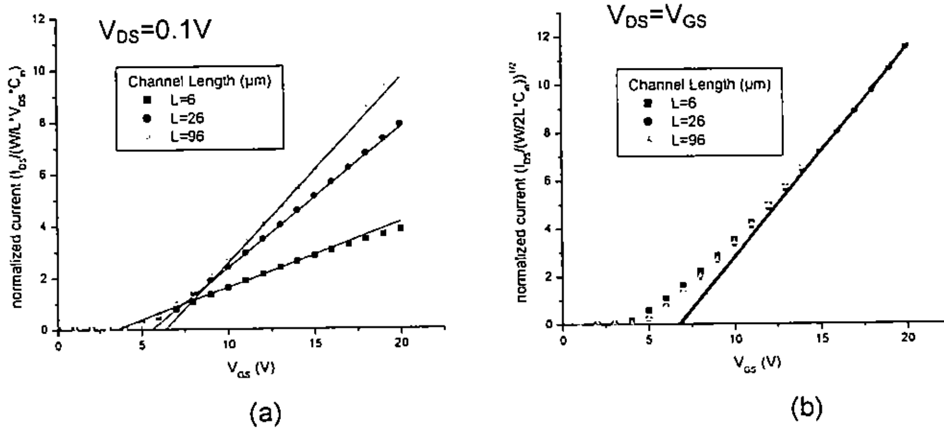

Figure 3.7 Normalized a-Si:H TFT transfer characteristics and fitting used for extraction of the field-effect mobility and threshold voltage in the (a) linear and (b) saturation regimes.

Examples of normalized TFT characteristics in linear and saturation regimes are shown in Figure 3.7a and b, respectively.

3.3.2 Extraction of Thin-Film Transistor Electrical Parameters

The most basic TFT characterization involves the extraction of field-effect mobility, threshold voltage, and subthreshold swing. To obtain meaningful extracted TFT electrical parameters, the fitting range must be chosen carefully to ensure that devices with different geometry, gate insulator characteristics, or measurement conditions are compared in the same operating states, which do not necessarily occur at comparable gate voltage ranges.

In the linear regime, i.e., for low drain voltage, the TFT apparent field-effect mobility μ_{FE} and threshold voltage V_T are deduced from the following equation, using the MOSFET gradual channel approximation:

$$\frac{I_{DS}}{V_{DS}C_i\ W/L} = \mu_{FE}\,(V_{GS} - V_T) \tag{3.16}$$

The fit of the experimental data to Eq. (3.16), as shown in Figure 3.7a, is performed around a fixed value of the normalized drain current $I_{DS}/(V_{DS}C_iW/L)$.

In the saturation regime (typically for $V_{DS} = V_{GS}$), the TFT field-effect mobility and threshold voltage are calculated from the following equation:

$$\frac{I_{DS}}{C_i W/2L} = \mu_{FE}(V_{GS} - V_T)^2 \tag{3.17}$$

The fit of the experimental data to Eq. (3.17), as shown in Figure 3.7b, is performed around a fixed value of the normalized drain current $I_{DS}/(C_i W/2L)$.

In addition, the normalized threshold voltage $V_T \times C_i$ should be used instead of the threshold voltage, to allow for comparison of devices with different gate insulator characteristics.

The subthreshold swing (S) is usually extracted from the TFT transfer characteristic in the subthreshold regime, using the following equation:

$$S = \left(\frac{d \log (I_D)}{dV_{GS}}\right)^{-1} \tag{3.18}$$

The fit of the experimental data to Eq. (3.18), as shown in Figure 3.8, is performed around a fixed value of $I_{DS}/(V_{DS}W/L)$. $I_{DS}/(V_{DS}W/L)$ can also be used in Eq. (3.18). From the value of the subthreshold slope, we can also calculate the equiva-

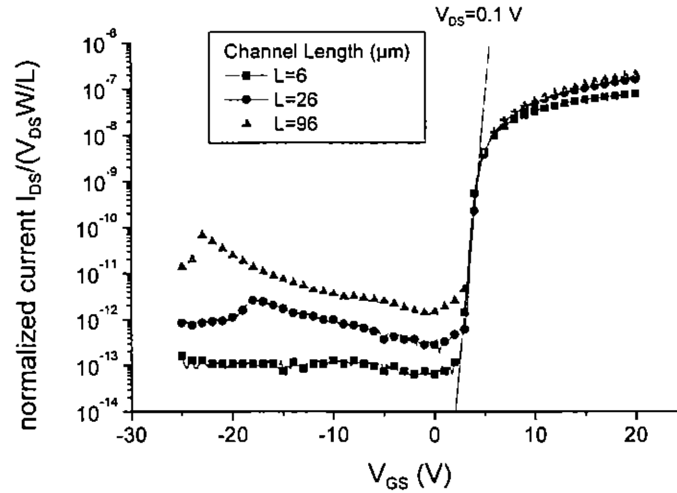

FIGURE 3.8 a-Si:H TFT transfer characteristics and fitting used for extraction of the subthreshold swing.

lent maximum density-of-states that can be present at the amorphous semiconductor/gate insulator interface [27]:

$$N_{ss}^{max} = \left(\frac{S \log(e)}{kT/q} - 1\right)\frac{C_i}{q} \tag{3.19}$$

where q is the electron charge, k is the Boltzmann constant, and T is the temperature. N_{ss}^{max} can be used to compare devices with different gate insulator characteristics.

In the linear regime, the MOSFET equation predicts that, for low V_{DS}, a linear $I_{DS} - V_{GS}$ characteristic should be observed. However, $I_{DS} - V_{GS}$ characteristics of TFTs often exhibit a nonlinear behavior inconsistent with the predictions of the MOSFET gradual channel equation, as seen, for example, in Figure 3.9. This deviation from the ideal MOSFET behavior [9,16,28,29] has been associated with dispersive transport in a-Si:H [30]. More precisely, the device model was modified to include an additional parameter, γ, representative of the $I_{DS} - V_{GS}$ nonlinearity at low V_{DS}, as follows:

$$I_{DS} = M(V_{GS} - V_T)^{\gamma}\, V_{DS} \tag{3.20}$$

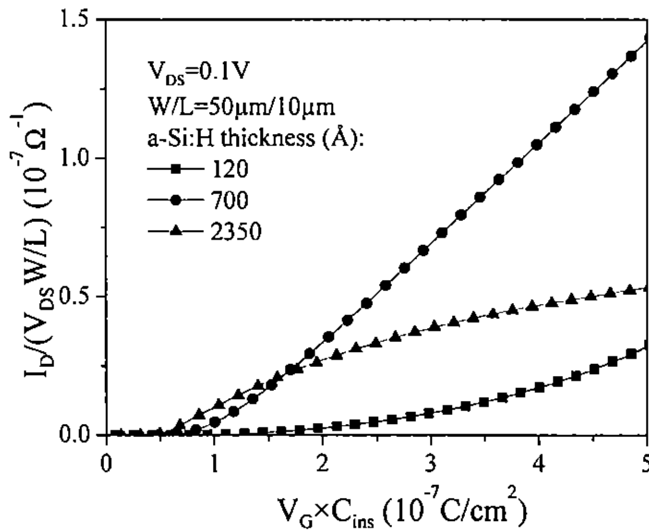

FIGURE 3.9 a-Si:H TFT transfer characteristics in the linear regime exhibiting significant nonlinearity.

where $M = \mu_{FE}C_i\ (W/L)$. The physical signification of γ is often given by

$$\gamma = 2\frac{T_0}{T} - 1 \tag{3.21}$$

where T_0 is the characteristic temperature of the amorphous semiconductor density-of-states distribution around the position of the Fermi level [16], i.e., typically the characteristic temperature of the conduction-band-tail states. The equation is valid for $T < T_0$. The nonideal situation of $\gamma > 1$ is associated with a high density of conduction-band-tail states, which can usually be attributed to variations of the Si–Si bond angles and distances in the amorphous semiconductor. However, γ can be significantly underestimated in the case of nonnegligible source and drain series resistances [31].

We should note that, when the TFT parameter extraction is performed using Eq. (3.20), the unit of the term $\mu_{FE}C_i\ (W/L)$ is $A/V^{\gamma+1}$ (instead of A/V^2 as in the case of the MOSFET-based equation) and consequently depends on the value of γ. Therefore, to ensure proper comparison between samples with different γ-values, the TFT field-effect mobility and threshold voltage are extracted using Eq. (3.16), i.e., based on the MOSFET gradual channel approximation. Eq. (3.20) was used separately for the extraction of the γ-parameter only.

3.3.3 Thin-Film Transistor Source/Drain Series Resistances

The complete analysis of a-Si:H TFT electrical performance also involves the extraction of the TFT source and drain series resistances, the intrinsic field-effect mobility, and intrinsic threshold voltage. The intrinsic a-Si:H TFT parameters are representative of the electrical characteristics of the conduction channel itself without the influence of the parasitic series resistances. They can be extracted by the well-known transmission line method (TLM) [32,33] using a series of TFTs with different channel lengths measured at a low source–drain voltage, so we can neglect the space-charge-limited currents (SCLC) effect.

The total TFT ON-resistance is:

$$R_T = \frac{V_{DS}}{I_{DS}} = r_{\text{ch}}\, L + 2R_{S/D} \tag{3.22}$$

where r_{ch} is the channel resistance per channel-length unit and $2R_{S/D}$ is the total (source + drain) series resistances, respectively. Using Eqs. (3.16) and (3.22), we can express the total TFT ON-resistance R_T as a function of the TFT apparent field-effect mobility and threshold voltage:

$$R_T = \frac{L}{\mu_{FE}\, C_i W (V_{GS} - V_T)} \tag{3.23}$$

The same equation applied to the ideal TFT (conduction channel only) lets us express the channel resistance as a function of the intrinsic mobility and threshold voltage, μ_{FEi} and V_{Ti}, which are representative of the conduction channel material, without the influence of the TFT series resistances:

$$r_{\text{ch}} = \frac{1}{\mu_{FEi}\, C_i W (V_{GS} - V_{Ti})} \tag{3.24}$$

The extraction of the TFT source and drain series resistances and intrinsic field-effect mobility and threshold voltages is rather straightforward using a series of TFTs with different channel lengths, as shown in Figure 3.10. We first plot the total TFT ON-resistance as a function of the TFT channel length for different gate voltages, ensuring that the TFT is in accumulation regime, and then we fit the experimental data to linear curves. This lets us obtain the TFT total series resistances ($R_S + R_D$) from the y-intercepts and the channel resistance per channel-length unit (r_{ch}) from the slopes. By plotting the reciprocal of r_{ch} as a function of the gate voltage and, once again, determining its linear fit, the x-intercept gives the intrinsic threshold voltage V_{Ti} and the slope yields the intrinsic field-effect mobility μ_{FEi} as indicated by Eq. (3.24).

The TFT series resistances are closely related to the overlap between source (or drain) contact and gate contact. The TFT drain current does not usually flow

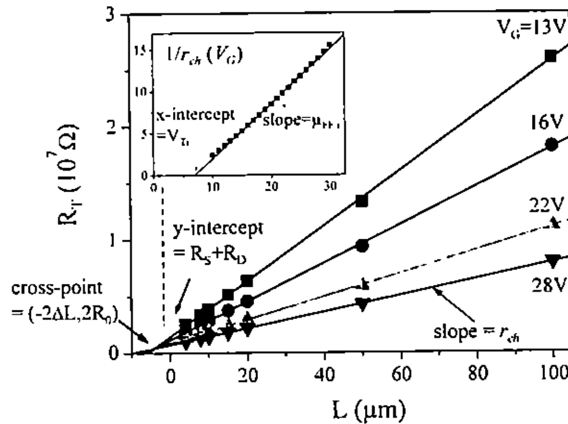

FIGURE 3.10 Illustration of the transmission line method used to extract the S/D series resistances and the a-Si:H TFT intrinsic parameters. The total ON-resistance R_T has been plotted as a function of the TFT channel length for different gate voltages. The inset shows the evolution of $1/r_{\text{ch}}$ with the TFT gate voltage. Symbols: experimental results; solid lines: linear fits. (Adapted from Ref. 26)

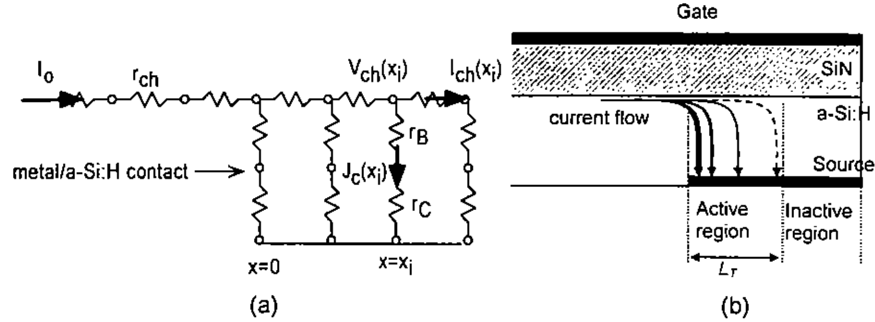

FIGURE 3.11 (a) Equivalent circuit near and above the a-Si:H TFT source electrode. (Adapted from Ref. 39.) (b) Representation of the characteristic length L_T. (From Ref. 23.)

through the whole source or drain contact but is more likely limited to a specific area of the contact [34–36]. More precisely, we can define the TFT characteristic length (L_T) representing the dimension (along the source–drain axis) of the effective contact area. Figure 3.11 illustrates the top-gate a-SI:H TFT cross section and simplified schematic circuit diagram at the source contact. At the source-electrode side, the change of the channel current above the source electrode can be expressed as

$$\frac{dI_{ch}(x)}{dx} = -WJ_c(x) \tag{3.25}$$

with

$$J_C(x) = V_{ch}(x)/r_{Ceff} \tag{3.26}$$

and

$$r_{Ceff} = r_B + r_C \tag{3.27}$$

where $I_{ch}(x)$ is the horizontal current in the channel (a-Si:H/a-SiN_x:H interface) at position x, $J_c(x)$ is the vertical current density at position x, $V_{ch}(x)$ is the electrical potential in the channel at position x, and r_B and r_C are the vertical bulk and contact resistivity (in Ω-cm^2), respectively.

The variation of $V_{ch}(x)$ along x can be expressed as

$$\frac{dV_{ch}(x)}{dx} = -I_{ch}(x)r_{ch} \tag{3.28}$$

Combining Eqs. (25), (26), and (27), we have

$$\frac{d^2V_{ch}(x)}{dx^2} = \frac{1}{L_T^2} V_{ch}(x) \tag{3.29}$$

with

$$L_T^2 = \frac{r_{Ceff}}{Wr_{ch}} \tag{3.30}$$

where L_T is the characteristic length of the source (drain) series resistance at a fixed V_{GS}.

The boundary conditions for Eq. (2.28) are

$$\left.\frac{dV_{ch}(x)}{dx}\right|_{x=0} = -I_0 r_{ch} \tag{3.31}$$

and

$$\left.\frac{dV_{ch}(x)}{dx}\right|_{x=d} = 0 \tag{3.32}$$

where I_0 is the total TFT drain-to-source current.

We can solve Eq. (3.29) for $V_{ch}(x)$ analytically:

$$V_{ch}(x) = I_0 r_{ch} L_T \frac{\cosh[(x - d)/L_T]}{\sinh(d/L_T)} \tag{3.33}$$

The series resistance $R_{S/D}$ (in ohms) at the source or drain contact can then be expressed as

$$R_{S/D} = \frac{V_{ch}(x = 0)}{I_0} = r_{ch} L_T \coth\left(\frac{d}{L_T}\right) \tag{3.34}$$

and

$$L_T = \frac{R_{S/D}}{r_{ch} \coth(d/L_T)} \tag{3.35}$$

The values of $R_{S/D}$ and r_{ch} are determined experimentally from Eqs. (3.22) and (3.24), respectively. Therefore, L_T can be calculated by solving Eq. (3.35) numerically. Furthermore, if $d/L_T >> 1$, Eq. (3.35) can be reduced to

$$L_T = \frac{R_{S/D}}{r_{ch}} \tag{3.36}$$

and from Eq. (3.30) we can obtain the effective contact resistance:

$$r_{Ceff} = WL_T^2 r_{ch} = \frac{WR_{S/D}^2}{r_{ch}} \tag{3.37}$$

It can be shown that, as expected for a-Si:H TFTs, r_{Ceff} and L_T vary with V_{GS} in

Eq. (3.35) through Eq. (3.37). Assuming that r_C is V_{GS} independent, this variation can be associated with a variation of series bulk resistivity (r_B) with V_{GS}. Thus, we can approximate the source/drain contact resistivity (in Ω-cm²) by

$$r_C = R_{C\mathrm{eff}}|V_{GS} >> 0 \tag{3.38}$$

if the bulk resistivity r_B is assumed to be negligible, as compared to r_C, at high V_{GS} for TFTs with thin a-Si:H layers. Taking this assumption into consideration, the r_C-value that we obtain (0.18 Ω-cm² for top-gate a-Si:H TFTs) is smaller than the one calculated by assuming a uniform conduction through the contact area (1 Ω-cm² for top-gate a-Si:H TFTs) [36]. This difference is associated with the difference between the characteristic length L_T and the source/drain contact width used in respective calculations of r_C. Therefore, the vertical current flow at the source (or drain) contact is effectively confined within a distance of about L_T from the edge of the contact.

The characteristic length L_T increases with the amorphous silicon thickness, the a-Si:H bulk density-of-states, and the source and drain contact resistances [23]. It is a critical parameter for designing TFTs. It is clear that, above the L_T-value, the contact dimension (i.e., the overlap between the source or drain contact and the gate contact) has no influence on the parasitic series resistances, since the current does not flow through the further part of the source or drain contact (inactive region). On the contrary, below L_T the whole contact area is active with respect to the current flow: The resistance is roughly proportional to the reciprocal of the contact dimension. Therefore, an increase in the contact dimension results in a reduction of the TFT series resistances and an improvement in the TFT electrical performance. However, we have to keep in mind that an increase of the overlap between the source or drain contact and the gate contact also yields to an increase in the TFT parasitic capacitances that can degrade the TFT performance, especially when used in active-matrix displays and detectors.

It has also been shown that the resistivity of the a-Si:H access region is closely associated with the band profile in the a-Si:H layer between the source (or drain) contact and the conduction channel [37] and therefore depends strongly on both the a-Si:H thickness and the a-Si:H density-of-states. If the a-Si:H density-of-states were constant throughout the electronic gap, the characteristic length of the band bending (potentials variations) would be the Debye length L_D, which can be simply approximated by the following equation:

$$L_D = \sqrt{\frac{\varepsilon_{\text{a-Si:H}}}{q^2 \times \text{density-of-states}}} \tag{3.39}$$

where q is the electron electric charge and $\varepsilon_{\text{a-Si:H}}$ is the amorphous silicon relative permittivity. Although the actual a-Si:H density-of-states is not constant throughout the electronic gap, the characteristic length L_D defined by Eq. (3.39) can still

be used to describe quantitatively the influence of a-Si:H thickness and density-of-states on the band profile.

The effect of the series resistances can also be partially represented as an increase in the apparent channel length: The total TFT ON-resistance is

$$\begin{aligned} R_T = \frac{V_{DS}}{I_{DS}} &= 2R_{S/D} + \frac{L}{\mu_{FEi}C_iW(V_{GS} - V_{Ti})} \\ &= 2R_0 + \frac{L + 2\,\Delta L}{\mu_{FEi}C_iW(V_{GS} - V_{Ti})} \end{aligned} \tag{3.40}$$

where ΔL is independent of the gate voltage and R_0 represents the limit of the source and drain series resistance for a very high gate voltage [32]. ΔL and R_0 are usually extracted from the R_T versus L curves, as shown in Figure 3.10: All the $R_T - L$ curves have a common cross point located slightly away from the y-axis [19,26,32], whose coordinates are ($x = -2\Delta L, y = 2R_0$). ΔL is associated with an effective channel length longer than the mask-specified channel length, i.e., the current path extending beyond the source/drain contact edges. It depends significantly on the source and drain contact resistances, as shown by the simulated results plotted in Figure 3.12.

The $I_{DS} - V_{DS}$ characteristics and their derivatives can also be used to evaluate qualitatively the effect of the source and drain series resistances. By plotting the derivative of the $I_{DS} - V_{DS}$ characteristics, we can better visualize the current crowding phenomenon that is associated with high source and drain series resistances. The presence of a significant current crowding results in an

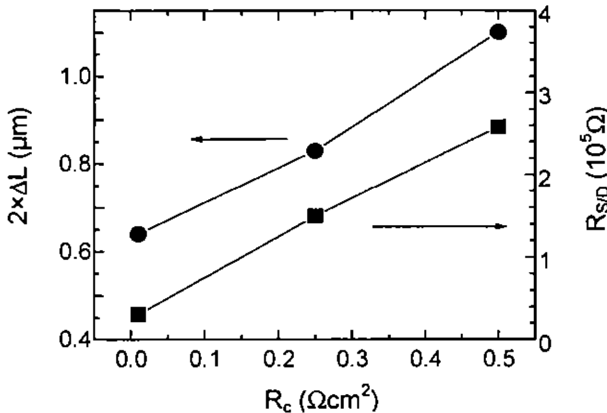

FIGURE 3.12 Simulated evolution of ΔL and $R_{S/D}$ as a function of the source/drain specific contact resistance. (Reprinted from Ref. 19 with permission from Elsevier Science.)

increase in the dI_{DS}/dV_{DS} curve for low V_{DS} values, while the absence of crowding yields a monotonic (decreasing) curve [32].

3.3.4 Gated Four-Probe Amorphous Silicon Thin-Film Transistors

3.3.4.1 Device Structure

Because of their staggered structure, TFTs often suffer from high source and drain series resistances that can affect their intrinsic channel performance, as described earlier. To accurately evaluate the a-Si:H TFT intrinsic properties without the influence of the parasitic series resistances, the gated four-probe TFT (GFP TFT) structure [19,38,39] has been developed by Chen et al. for the first time. This structure can also be called a five-terminal (FT) TFT, an intrinsic point probe MOSFET, or a Kelvin probe TFT.

The GFP TFT is a TFT with two additional narrow electrodes placed between the source and drain contacts (see Fig. 3.13). Such a structure is expected to allow for the evaluation of the potential difference along the conduction channel, assuming that the potential difference is the same at the conduction channel

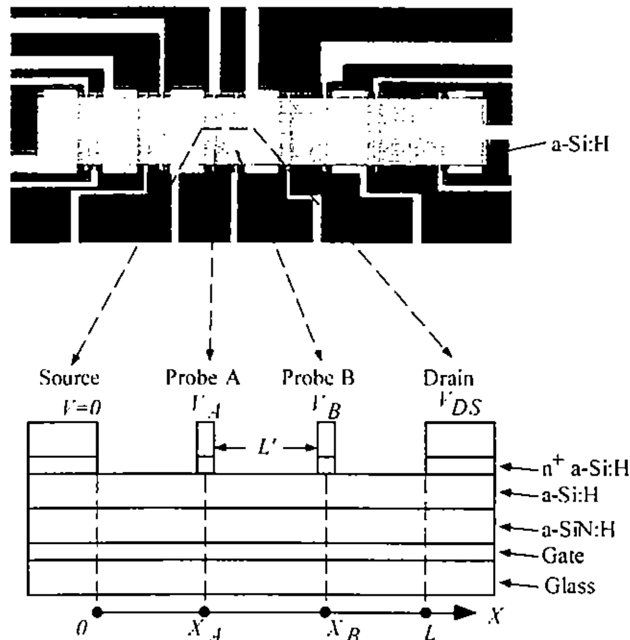

Figure 3.13 Top and cross-sectional views of the GFP a-Si:H TFT structure. (From Ref. 38.)

interface (amorphous semiconductor/gate insulator) and at the back interface (passivation layer/amorphous semiconductor). We have shown that, indeed, GFP-TFTs can be used to accurately study TFT conduction channel intrinsic properties [38].

The gradual channel approximation in the linear region is used to describe the a-Si:H TFT electrical characteristics:

$$G = \frac{I_{DS}}{V_{DS}W/L} = \mu_{FE}C_i(V_{GS} - V_T) \tag{3.41}$$

where G is the normalized channel conductance. For the GFP a-Si:H TFT structure, the $G' - V_{GS}$ characteristics are derived from

$$G' = \frac{I_{DS}}{(V_B - V_A)W/L'} = \mu_{FEi}C_i(V'_{GS} - V_{Ti}) \tag{3.42}$$

where G' is the effective normalized channel conductance, V_A and V_B are the potential for the two inner probes; $V_{GS}' = V_{GS} - (V_B + V_A)/2$ is the effective gate bias, and $L' = (X_B - X_A)$ is the GFP effective channel length. Since probes A and B sense only the potential, V_A and V_B are the true potentials at the back channel and we can assume that the difference $V_A - V_B$ is the same as the corresponding potential difference in the conduction channel. Hence, by using the GFP a-Si:H TFT structure, intrinsic field-effect mobility (μ_{FEi}), intrinsic threshold voltage (V_{Ti}) and channel conductance activation energy (E_{act}) can be extracted from Eq. (3.42), without the influence of the TFT source/drain series resistances.

3.3.4.2 Bidimensional Numerical Simulation of Amorphous Silicon Gated Four-Probe Thin-Film Transistors

The 2D Semicad Device simulation program previously described was used to numerically study the effect of the series resistances on a-Si:H TFT and GFP a-Si:H TFT characteristics [38,40]. The $G - V_{GS}$ and $G' - V'_{GS}$ characteristics for a-Si:H TFT and GFP a-Si:H TFT structures have been simulated for different R_C. Figure 3.14 shows the evolution of the extracted field-effect mobility as a function of the channel lengths for three different R_C values for a-Si:H TFT and GFP a-Si:H TFT structures. As expected, the field-effect mobility of the conventional TFT decreases with decreasing channel length and increasing R_C values. On the other hand, since R_C has no influence on $G' - V'_{GS}$ characteristics of the GFP a-Si:H TFT structure, the field-effect mobility does not change with the GFP TFT effective channel length.

The electrical characteristics of real GFP TFTs have been studied by adding two additional probes (A and B) to the standard TFT design. It is assumed that

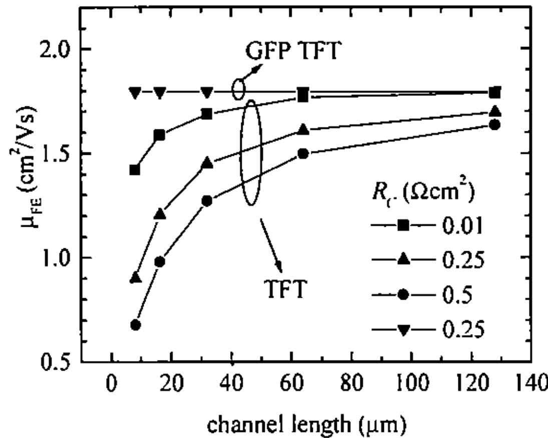

FIGURE 3.14 Simulated evolution of the field-effect mobility and the threshold voltage as a function of the channel length for a-Si:H TFT and GFP a-Si:H TFT structures having different R_c values. (From Ref. 15.)

these contacts are ohmic and that no current flows through these probes. The GFP and conventional TFT conductances (G' and G) were calculated using the same equations that have been used for experimental data. It has been verified that, for the typical a-Si:H thicknesses used in TFTs, the potential difference between the probes was similar to the potential difference in the conduction channel, although some differences were observed for very thick films (semiconductor thickness larger than 2000 Å).

In addition, the simulations have shown that the probe widths have to be less than 4 μm, typically, and the distance between probes and source/drain contacts larger than 1 μm, typically, to prevent any modification of the TFT characteristics. For larger probe widths, a significant electric field fringing effect is observed, resulting in a higher conductance for the TFT itself [40]. A similar effect was observed for distances between probes and S/D contacts shorter than 1 μm, typically. However, it should be noted that, for the typical GFP TFT design (probe width ~ 2 μm, distance probes—*S/D* about 10 μm), the electrical field fringing effect can be neglected and we can assume that the two inner probes do not affect the TFT electrical behavior.

The GFP TFT structure can be used to investigate the effect of the a-Si:H density-of-states on the TFT intrinsic electrical performance. An increase in the density of conduction-band-tail (CBT) states result in a reduction of the field-

effect mobility and an increase in the threshold voltage, as shown in Figure 3.15. It also results in an increase in the γ-coefficient associated with the transfer characteristics non-linearity. However, γ-values extracted for conventional TFTs can apparently be reduced by the TFT parasitic resistances and can therefore lead to incorrect TFT analysis. Figure 3.16 shows that $\gamma = 1$ can be observed for a TFT with a high density of CBT states and high source/drain series resistances. In contrast, the GFP TFT structure allows for the accurate estimation of γ, converging toward 1 for low values of the CBT density-of-states. In contrast, an increase of the density-of-deep-gap states results only in an increase of the threshold voltage, as is clearly seen in Figure 3.17. It has no effect on the TFT intrinsic field-effect mobility or γ. Therefore, μ_{FE} and γ are associated mainly with the conduction band-tail characteristic energy. The GFP TFT structure can be used to distinguish between the changes due to a variation in the amorphous semiconductor density of conduction-band-tail states from the ones associated with the density of deep-gap states.

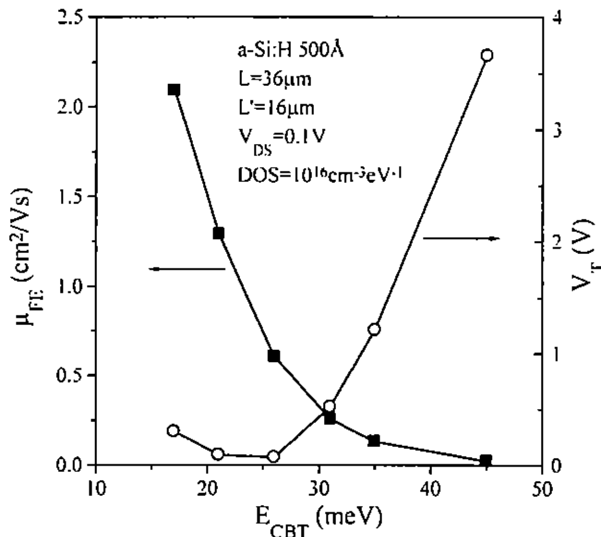

FIGURE 3.15 GFP a-Si:H TFT field-effect mobility and threshold voltage in linear regime as a function of the characteristic energy of the a-Si:H conduction band tail. (From Ref. 40, with permission from Society for Information Display.)

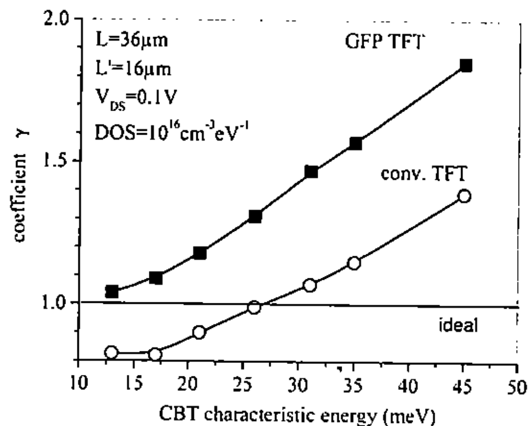

FIGURE 3.16 Coefficient γ as a function of the a-Si:H conduction-band-tail characteristic energy. (From Ref. 40, with permission from Society for Information Display.)

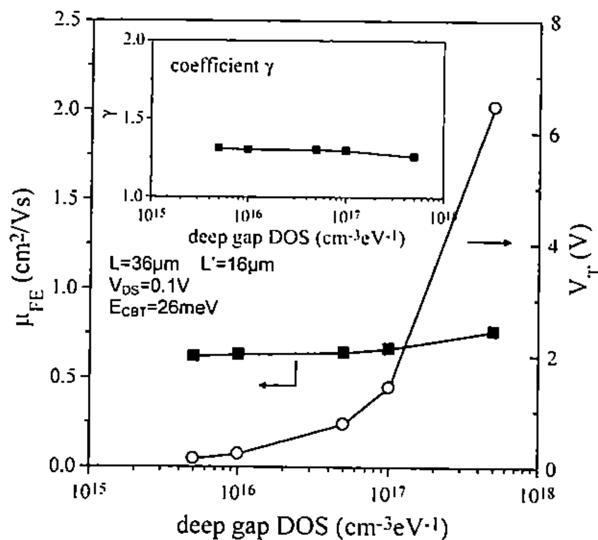

FIGURE 3.17 GFP TFT field-effect mobility and threshold voltage in the linear regime as a function of the density of deep-gap states. The inset shows the variation of γ with the density of deep-gap states. (From Ref. 40, with permission from Society for Information Display.)

3.3.4.3 Gated Four-Probe Thin-Film Transistor Experimental Results

To test the GFP a-Si:H TFT structure experimentally, a-Si:H TFT and GFP a-Si:H TFT structures were fabricated on the same Corning 7059F glass substrate in the same processing run [38]. The $G' - V_{GS}$ characteristics for a-Si:H TFT and GFP a-Si:H TFT having different channel lengths (L or L') are shown in Figure 3.18. For a-Si:H TFTs, in the linear region, a lower conductance is observed for a shorter-channel-length device because of the effect of the TFT source/drain series resistance. For the GFP a-Si:H TFT, as expected, no channel length dependence is observed in the $G' - V_{GS}$ characteristics. Similarly, high source and drain contact resistances result in significant degradation of the conventional TFT conductivity, while the GFP TFT conductivity is not affected [40]. Finally, a thicker a-Si:H layer (3000 Å) also causes a strong reduction in the source–drain conductance of the a-Si:H TFT due to a higher S/D series resistances while GFP TFT characteristics are nominally independent of the a-Si:H film thickness [39].

3.3.5 Amorphous Silicon Thickness Effects

The a-Si:H film thickness has a significant effect on the a-Si:H TFT characteristics, mostly in the ON-state and subthreshold regime. One does not observe any notable a-Si:H film thickness effect on the TFT OFF-current, as shown in Figure

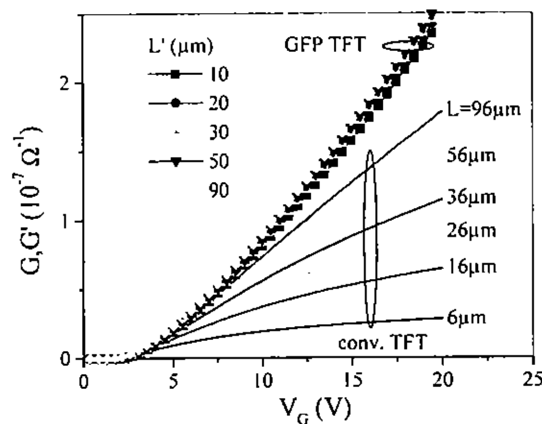

FIGURE 3.18 Normalized conductance versus gate voltage curves measured for conventional and GFP TFTs, for different TFT channel lengths. (Adapted from Ref. 39.)

3.19, but one clearly notices the thickness dependence of the TFT ON-state parameters in the linear regime. When the thickness of the amorphous silicon layer increases, the following changes occur:

1. Improvement of the subthreshold slope (inset Fig. 3.19)
2. Increase of the apparent field-effect mobility for thin a-Si:H layers (Fig. 3.20)
3. Reduction of the apparent field-effect mobility for thick a-Si:H layers (Fig. 3.20)
4. Increase of the intrinsic field-effect mobility (for all the a-Si:H thicknesses, Fig. 3.20)
5. Reduction of the threshold voltage (Fig. 3.20)
6. Reduction of the γ-coefficient (Fig. 3.21)

The evolution of the subthreshold slope and the intrinsic field-effect mobility in the linear regime suggests that the electronic quality of the amorphous silicon (in terms of density-of-states) is improved, while the reduction of the TFT apparent field-effect mobility observed in the case of a very thick a-Si:H film results most likely from a stronger influence of the parasitic access resistances.

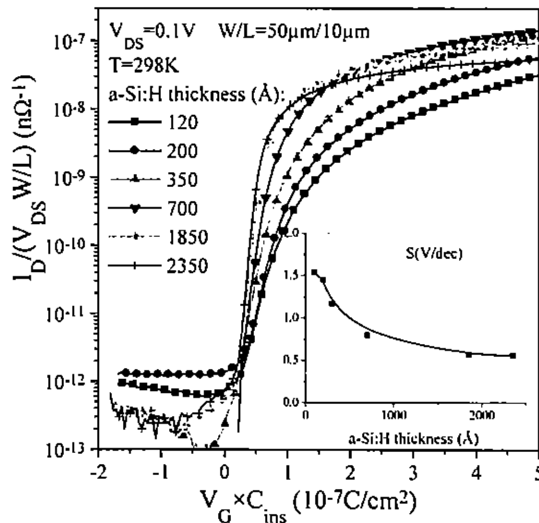

FIGURE 3.19 TFT transfer characteristics measured in the linear regime (V_{DS} = 0.1 V) for 10-μm-long top-gate a-Si:H TFTs with different a-Si:H thicknesses. The inset shows the evolution of the subthreshold swing as a function of the a-Si:H thickness. (From Ref. 26.)

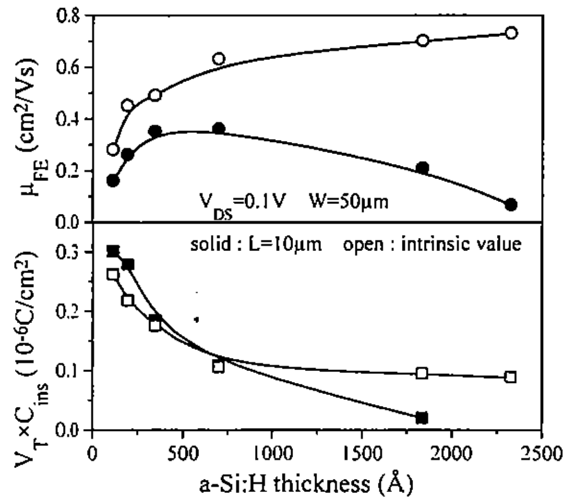

Figure 3.20 Variations of the a-Si:H TFT ON-state parameters in the linear regime as a function of the a-Si:H thickness. Solid symbols show apparent field-effect mobility and normalized threshold voltage for 10-μm-long TFTs and open symbols show intrinsic field-effect mobility and normalized threshold voltage. (From Ref. 26.)

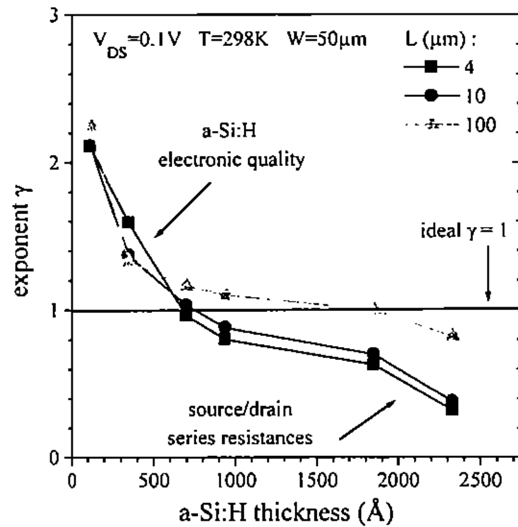

Figure 3.21 Exponent γ variations as a function of the a-Si:H thickness for different TFT channel lengths. (From Ref. 26.)

The reduction of the threshold voltage is probably due to a weaker influence of the back interface when the amorphous silicon thickness increases. The decrease of the γ-exponent with increasing a-Si:H thickness suggests a lower density of conduction-band-tail states present in thicker a-Si:H films. The results obtained in the saturation regime exhibited the same trend as the ones obtained in the linear regime: The TFTs made from thicker a-Si:H films have better electrical performance (higher field-effect mobility and lower threshold voltage) than the thinner ones. This is consistent with the idea that the amorphous silicon quality is improved when the film thickness increases. As shown in Figure 21, for a very thick a-Si:H film and short TFT channel length, higher source/drain series resistances result in a low γ-value, i.e., less than 1. The increased effect of the source/drain series resistances has been confirmed by the analysis of TFT output characteristics and their derivatives [26]: Current crowding was much more significant for thicker a-Si:H films. In addition, the series resistivity r_{ceff} increased with the a-Si:H film thickness, which confirms the significant effect of the access region between the source (or drain) contact and the conduction channel on the TFT S/D series resistances [37].

As explained earlier, the increase of the amorphous silicon thickness first results in an improvement of the a-Si:H TFT electrical performance, due to a better material electronic quality; then, for thicker a-Si:H layers, the access resistances become more and more significant and degrade the TFT electrical performance. Thus, it is necessary to find a compromise between amorphous semiconductor quality and source and drain access resistances. We can define an optimum amorphous silicon thickness as the one that results in the highest apparent field-effect mobility (Fig. 3.22), which depends on the electronic quality of the material and on the TFT source and drain series resistances. Similarly, an optimum value of the a-Si:H thickness can be defined, from the evolution of the TFT field-effect activation energy (E_{act}), as a function of the film thickness. It is well established that E_{act} depends on both the a-Si:H electronic quality and the source and drain series resistances (Fig. 3.23). We can see from Figures 3.22 and 3.23 that the TFT field-effect mobility and field-effect activation energy are optimized for similar values of the a-Si:H thicknesses. Also, we can notice in Figures 3.22 and 3.23 the clear dependence of the optimum a-Si:H thickness on the TFT channel length, connected to the stronger influence of the source and drain series resistances on shorter-channel TFTs. In comparison with long-channel TFTs, the degradation of short-channel TFT electrical performance with increasing a-Si:H thickness clearly appears for thinner a-Si:H layers. Typically, for these devices the optimum thickness for a 100 μm-long TFT is above 1000 Å, while the apparent field-effect mobility of a 10-μm-long TFT starts degrading for a-Si:H films thicker than 500 Å. The optimized a-Si:H thickness for short-channel TFTs, such as the ones used in AMLCDs, is below 500 Å, which is comparable to the a-Si:H thickness used for bottom-gate trilayer a-Si:H TFTs. This value is signifi-

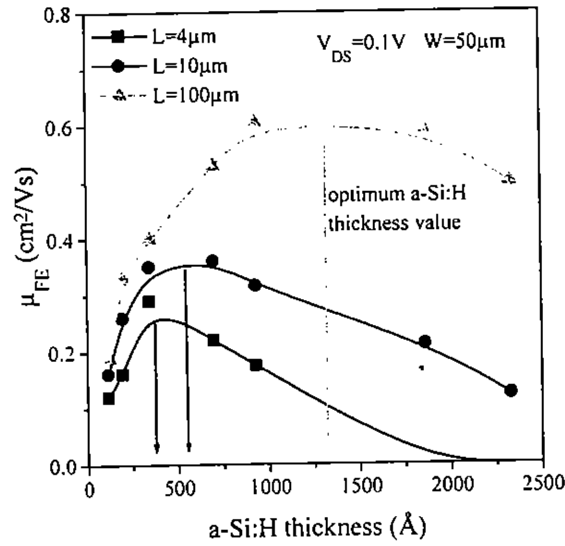

FIGURE 3.22 Variations of the a-Si:H TFT apparent field-effect mobility with a-Si:H thickness for different TFT channel lengths. (From Ref. 26.)

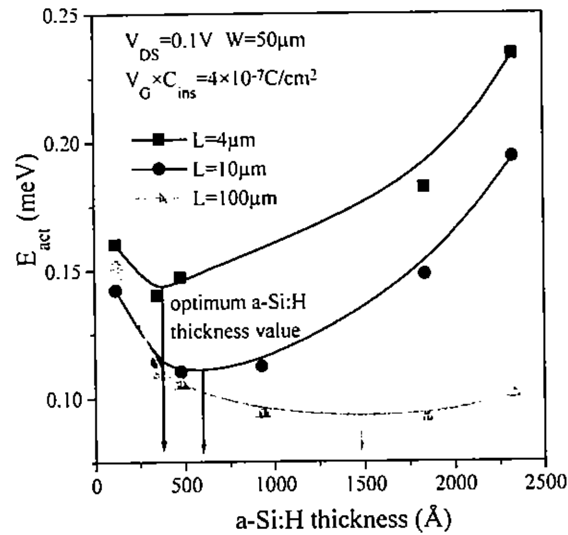

FIGURE 3.23 Variations of the a-Si:H TFT field-effect activation energy with a-Si:H thickness for different TFT channel lengths. (From Ref. 26.)

cantly smaller than the typical amorphous silicon thickness used for back-channel-etched TFTs, which is about 1500 Å.

3.3.6 Amorphous Silicon Thin-Film Transistor Under Illumination

To analyze the photosensitivity of a-Si:H TFTs in detail, we define the ratio between TFT drain current under illumination and in the dark [41]:

$$R_{L/D} = \frac{I_{DSillum}}{I_{DSdark}} \tag{3.43}$$

Figure 3.24 shows the TFT transfer characteristics measured in the dark and under illumination (white light, halogen bulb). The typical variations of $R_{L/D}$ with the TFT gate voltage are also shown in this figure. We can clearly see a peak corresponding to the TFT weak-accumulation regime, typically observed for small, positive gate voltages. In the strong-accumulation regime, the TFT current ratio decreases, as expected, because of the dominant effect of the gate voltage on the concentration of accumulated carriers. In the OFF-state, $R_{L/D}$ is significantly higher than in the ON-state, but still several decades lower than the peak value. The existence of the peak in the weak-accumulation regime can be understood by looking at the TFT transfer characteristics (Fig. 3.24). Because of the subthreshold slope change under illumination, we can identify a small gate

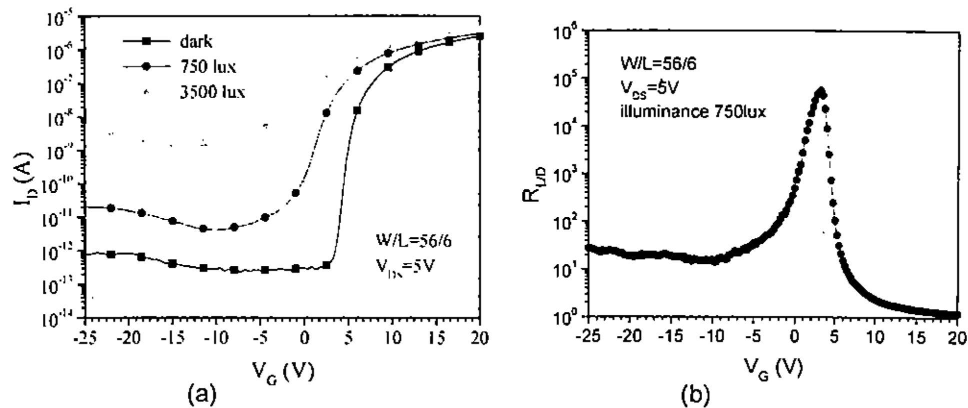

FIGURE 3.24 (a) Measured a-Si:H TFT transfer characteristics in the dark and under white-light illumination. (b) Typical behavior of the $R_{L/D}$ ratio between the TFT drain current under illumination and in the dark as a function of the TFT gate voltage, under white-light illumination. (From Ref. 41.)

voltage range for which the TFT is in the OFF-state in the dark and almost in the ON-state under illumination. This gate voltage range will therefore provide the highest $R_{L/D}$ ratio.

$R_{L/D}$ does not significantly depend on the drain voltage, ranging from 0.1 to 15 V. In the ON-state, the TFT current is proportional to the channel width and roughly inversely proportional to the channel length, neglecting the S/D series resistances. In the OFF-state in the dark, the TFT OFF-current is usually independent of channel width and channel length. We believe that this is due to a very low value of the TFT OFF-current in the dark: What we measure might be either measurement noise or transient current, in which other mechanisms are involved. When the TFT is under illumination, the carrier concentration is increased and the OFF-state conduction mechanisms are similar to the ON-state situation; the current is therefore again proportional to the channel width and inversely proportional to the channel length. Consequently, the peak value of $R_{L/D}$ increases with increasing channel width and with decreasing channel length.

The $R_{L/D}$ peak value can be as much as two to three orders of magnitude above the current ratio in the TFT OFF-state and could therefore be used very easily to detect the presence of light, even at low light intensities. We can clearly see in Figure 3.25a that the $R_{L/D}$ peak is significant even for very low illuminance values. The variations of $R_{L/D}$ (at $V_G = 1$ V) with the illuminance (IL) are shown in Figure 3.25b and clearly exhibit a power-law dependence; e.g., $R_{L/D} \propto IL^{\gamma}$, with $\gamma = 0.7$. Similar behavior was reported in the literature for the dependence of a-Si:H photoconductivity on illuminance. However, we should note that the $R_{L/D}$ peak is quite narrow, with a typical width at half height of a few volts or less. Consequently, the $R_{L/D}$ peak value strongly depends on the considered gate voltage, and a slight shift of the TFT transfer characteristic could result in erroneous values. The peak ratio in the low-accumulation regime can therefore be used to detect the presence of light but not to accurately quantify the light intensity. The OFF-regime, in which $R_{L/D}$ is much less sensitive to the gate voltage, would be more appropriate for this purpose.

The effect of the illumination wavelength on the TFT photosensitivity has also been studied. Two types of measurements were performed using monochromatic light at different wavelengths: constant optical power density (1.5×10^{-4} W/cm^2) and constant optical flux (6×10^{14} photons/cm^{2}s). The results in both cases are quite similar: A significant increase of the TFT photosensitivity with increasing photon energy was observed. This behavior is clearly associated with the absorption curve of amorphous silicon [41].

Finally, the effect of the TFT operation temperature was investigated, using monochromatic light ($\lambda = 620$ nm, $P = 77$ μW) to avoid any parasitic heating of the sample that can occur under white-light illumination [41]. From the analysis of the TFT operation, we have concluded that, for the same gate voltage, the TFT current increases with temperature much faster in the dark (OFF-state) than

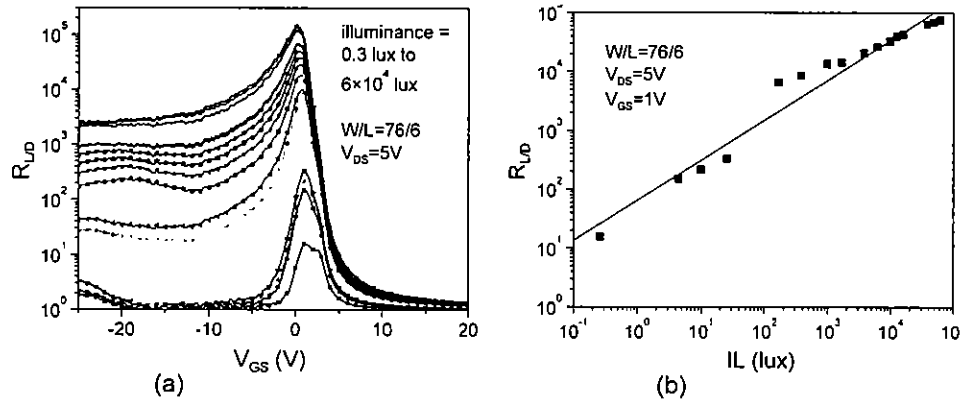

FIGURE 3.25 (a) $R_{L/D}$ as a function of the a-Si:H TFT gate voltage, for different white-light intensity values. (b) $R_{L/D}$ (for V_G = 1 V) as a function of the illuminance (IL). Symbols show experimental data; the solid line shows the fit to a power-law behavior, with an exponent $\gamma \sim 0.7$. (From Ref. 41, with permission from Society for Information Display.)

under illumination (weak-accumulation regime). We can therefore expect $R_{L/D}$ to decrease with increasing temperature, which was experimentally confirmed [41].

3.4 ADVANCED HYDROGENATED AMORPHOUS SILICON THIN-FILM TRANSISTOR STRUCTURES

3.4.1 High-Performance Back-Channel-Etched Hydrogenated Amorphous Silicon Thin-Film Transistors

To improve productivity and to lower the fabrication costs of AMLCDs, there was a need to enhance the throughput and operation up-time of plasma-enhanced chemical vapor deposition (PECVD) tools used in the fabrication of a-Si:H TFTs. This should be achieved without sacrificing a-Si:H TFT electrical performance. One method consists of increasing the rate of deposition of the PECVD materials. Different methods, such as very high-frequency plasma [42], high pulsed-RF power density [43], helium dilution [44], and the unique design of electrodes for efficient ionization in the multichamber system for cost-effective manufacturing [45,46], have been developed to produce a-Si:H film with a high deposition rate. Among these different technologies, only a very high-frequency (60 MHz) PECVD [47] and a multichamber PECVD [45,46] systems approach have been

used in the production of a-Si:H TFTs. For very high-frequency (60 MHz) PECVD, it has been reported [47] that a-Si:H TFT having a high field-effect mobility (μ_{FE}) (1.1 cm^2/V-s) can be fabricated from high-deposition-rate materials. However, in another high-frequency (40 MHz) PECVD system of a similar design, a slightly lower mobility (0.7 cm^2/V-s) has been obtained [48]. At the same time, a-Si:H TFTs exhibiting $\mu_{FE} \approx 0.8$ cm^2/V-s were fabricated from high-growth-rate materials [49] produced in a multichamber PECVD system.

3.4.1.1 Back-Channel-Etched Device Structure and Fabrication Process

The most commonly used TFTs have a bottom-gate (BG) back-channel-etched (BCE) structure, shown in Figure 3.26. The thicknesses of N-rich hydrogenated amorphous silicon nitride (a-$SiN_{1.5}$:H), intrinsic a-Si:H, and *P*-doped (n^+) a-Si:H are 2480, 2000, and 500 Å, respectively. The channel length is defined by using the source/drain metal (3000-Å-thick Mo) as a mask. The channel width and length of typical TFTs are 116 and 32 μm, respectively. Using this structure, high-field-effect-mobility TFTs have been fabricated [50] from high-deposition-rate materials deposited at 320°C in a 13.6-MHz AKT 1600 multichamber PECVD system. The a-Si:H was deposited under the following conditions: silane flow = 250–500 sccm, hydrogen flow = 2800 sccm, pressure = 2–4 torr, and RF power = 150 W. The microstructure of the high-deposition-rate materials was similar to the one obtained for low-rate PECVD films [51]. The materials used in these TFTs have the following properties: (1) a-Si:H deposition rate is 50 nm/min, dark conductivity is about 2.6×10^{-11} Ω^{-1} cm^{-1}, activation energy is 0.94 eV, Tauc optical bandgap is 1.78 eV, and hydrogen content is about 3×10^{21} cm^{-3}; (2) a-$SiN_{1.5}$:H growth rate is 190 nm/min, etching rate in oxide etch solution is 61 nm/min, Tauc optical bandgap is 5.0 eV, dielectric constant is 7.0 (measured at 1-MHz frequency), and hydrogen content is about 1.9×10^{22} cm^{-3}; (3) n^+ a-Si:H growth rate is 60 nm/min, film resistivity is 41 Ω-cm, activation energy is 0.2 eV, Tauc optical bandgap is 1.74 eV, and Mo/n^+ a-Si:H contact resistance (R_c) is 0.25 Ω-cm^2.

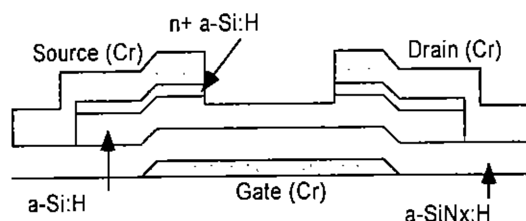

Figure 3.26 Cross section of BCE a-Si:H TFT.

3.4.1.2 Back-Channel-Etched Device Electrical Performance

Figure 3.27a shows the TFT output characteristics for various gate voltages. No current-crowding effect is observed at small drain voltages, suggesting good electrical/ohmic quality of the source/drain contacts. Figure 3.27b shows the TFT transfer characteristics for various V_{DS}. At V_{DS} = 10 V, the ON- to OFF-current ratio exceeds 10^7 and the OFF-current is less than 10^{-12} A. In the linear regime (V_{DS} = 0.1 V) the subthreshold swing (S) is about 0.3 V/dec, corresponding to a maximum density of deep-gap states, localized at or near the a-SiN_x:H/a-Si:H interface, $N_{SS}^{max} = 8 \times 10^{11}$ $cm^{-2}eV^{-1}$ [27]. The TFT field-effect mobility is 1.45 and 1.15 cm^2/V-s in the saturation and linear regimes, respectively. The TFT field-effect mobility is channel length dependent, as expected, and the intrinsic TFT field-effect mobility is about 1.60 cm^2/V-s. This high field-effect mobility value is in agreement with a low density of the interface states, mentioned earlier. The TFT threshold voltage is 2.0 and 1.9 V in the saturation and linear regimes, respectively. This low V_T is also consistent with a low density of interface states. From the temperature dependence of the $I_{DS} - V_{GS}$ characteristics, the field-effect activation energy was calculated as a function of V_{GS} [50]: The activation energy is on the order of 50 meV at V_{GS} = 20 V. This activation energy value corresponds to a slope of conduction-band-tail states of about 27 meV.

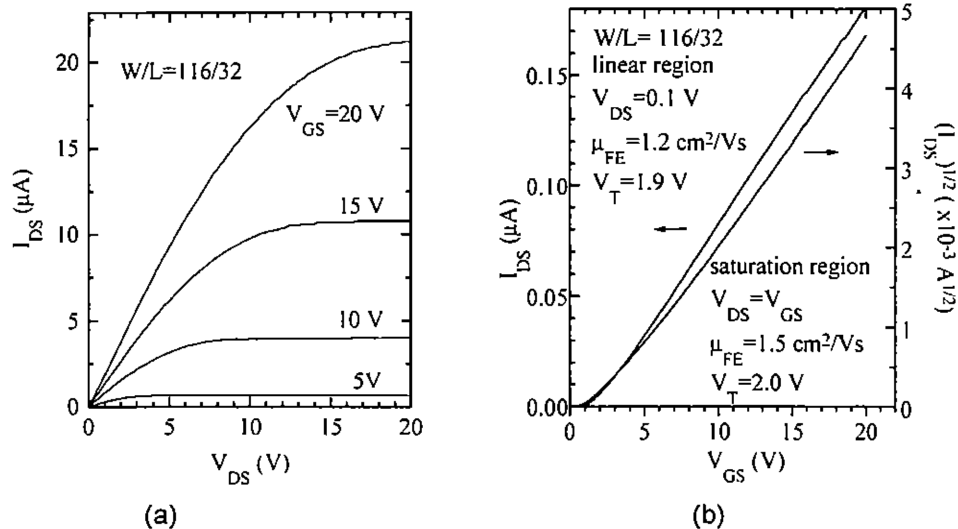

FIGURE 3.27 (a) Output and (b) transfer characteristic of a high-performance BCE a-Si:H TFT. (From Ref. 50.)

3.4.2 Gate-Planarized Hgdrogenated Amorphous Silicon Thin-Film Transistor

The reduction of gate busline RC propagation delay and the enhancement of the pixel-electrode aperture ratio are very important for large-area, high-resolution, and low-power AMLCDs. Gate planarization technology [52,53] allows for the use of thick and, consequently, low-resistivity gate electrodes (Al or Cu) without having problems associated with electrode step coverage, taper edge definition [54,55], hillock formation when pure Al is used, or Cu-etching difficulties [56].

3.4.2.1 Gate-Planarized Device Structure and Fabrication Process

The fabrication process of the back-channel-etched (BCE) gate planarized (GP) a-Si:H TFTs is very similar to that of the conventional BCE a-Si:H TFTs; no additional photolithography step is needed. These GP-TFTs were fabricated on Corning 7059 glass substrate. First, a 5500-Å-thick Cr layer was prepared via DC sputtering. After the gate electrode/busline definition, a benzoclybutene (BCB, $\varepsilon_r = 2.4$) layer about 6000 Å thick was spin-coated directly over the Cr gate lines without any adhesion/barrier metal layer. After spin-coating, the BCB was cured in an N_2 convection oven at 250°C for 1 hr. Following the BCB curing, hydrogenated amorphous silicon nitride (a-SiN_x:H), intrinsic (i) and P-doped (n^+) a-Si:H films, having thicknesses of 500, 2000, and 600 Å, respectively, were deposited by PECVD at 250°C. After the active island definition, the gate vias composed of a-SiN_x:H and BCB layers were defined by reactive ion etch (RIE) using a CF_4/O_2 gas chemistry. A 3500-Å-thick Cr film was used to fabricate the source/drain (S/D) contact electrodes. After wet patterning of the S/D electrodes, the back-channel-etch of the n^+- and i-a-Si:H layers was done by RIE using a CCl_2F_2/O_2 gas chemistry. The gate insulator capacitance per unit area was 10^{-8} F/cm^2.

The electrical properties of BCB, such as its dielectric strength and current leakage induced by electric-field bias and the interface properties with c-Si, have been evaluated from metal–insulator–metal (MIM) and metal–insulator–semiconductor (MIS) structures, respectively. The leakage current density is about 3×10^{-7} A/cm^2 at an electric field of 2 MV/cm. This leakage current density is about an order of magnitude higher than typical values found for a high-quality nitrogen-rich a-SiN_x:H film [57]. A higher leakage current found in the BCB material can be associated with its smaller-energy band gap (~3.9 eV), in comparison with the PECVD a-SiN_x:H films (~5.3 eV) [51]. Carrier injection through the BCB layer by Schottky and/or Frenkle–Poole emission can be responsible for this leakage current [58]. It has also been observed that when BCB is in direct contact with the c-Si, serious trapping and detrapping can occur under a high electric field. This may not be acceptable for electronic device applications. From

an analysis of MIS structure characteristics, it appears that a carrier injection barrier is needed when the BCB is in direct contact either with the amorphous semiconductor active layers or metal contacts.

Figures 3.28a and b show SEM photographs of the conventional and the GP TFT-array structures, respectively. In Figure 3.28a, clear steps of the source/drain electrodes over the gate-electrode edges and the busline crossover edges

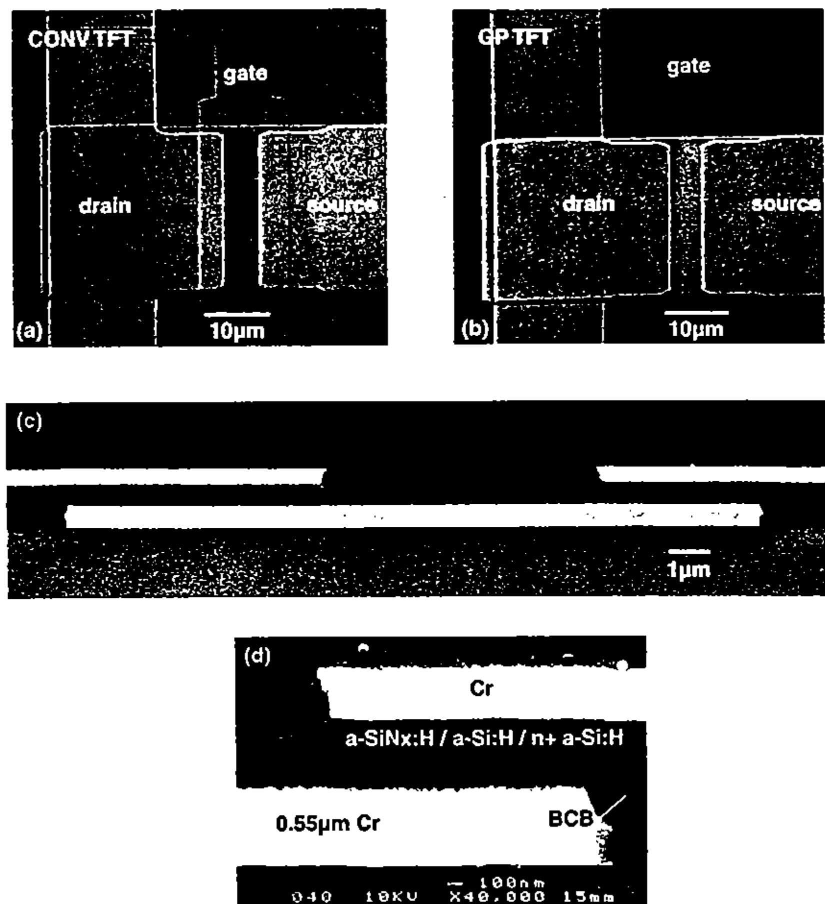

FIGURE 3.28 SEM photographs of (a) the conventional (CONV) and (b) the gate-planarized (GP) a-Si:H TFT structures. (c) Cross-sectional view of the GP-TFT. (d) Enlargement of the GP-TFT cross section in the source–gate overlap region. (Adapted from Ref. 52.)

can be seen for a thin (~800-Å-thick) gate electrode. In contrast, in Figure 28b, almost no steps are detected over an even thicker gate electrode (~5500 Å thick). Figures 3.28c and d show the cross section of the GP-TFT and the enlargement of the GP-TFT (L = 6 μm) in the source–gate overlap region, respectively. From this figure, it is clear that very good planarization of the thick-Cr-gate electrode has been achieved by the BCB layer. Even though the Cr electrode sidewalls are very rough (this most often occurs in the wet etching process), as shown in Figure 3.28d, the BCB layer can still completely fill the region adjacent to the sidewall areas without any void formation, and thus make it possible to produce a smooth PECVD a-SiN_x:H layer over the gate electrode corners. This excellent filling property of the BCB layer can thus ensure that no porous a-SiN_x:H layer is developed at the gate electrode corners and the dielectric defects caused by the subsequent wet etchant attack can be reduced. Therefore, there is no step coverage problem of the gate insulator over such a thick gate electrode structure. In addition to Cr gate metal, this technology can be applied to different gate metallurgies, such as Cu [59].

3.4.2.2 Gate-Planarized Thin-Film Transistor Electrical Performance

Figure 3.29 shows the GP-TFT (W/L = 56/6) output and transfer characteristics for different source–drain voltages (V_{DS} = 0.1, 1, and 10 V). For V_{DS} = 10 V, an ON- to OFF-current ratio of about 10^7 can be obtained. For V_{DS} = 0.1 V, the subthreshold swing (S) is about 0.43 V/dec. From this S-value, the calculated

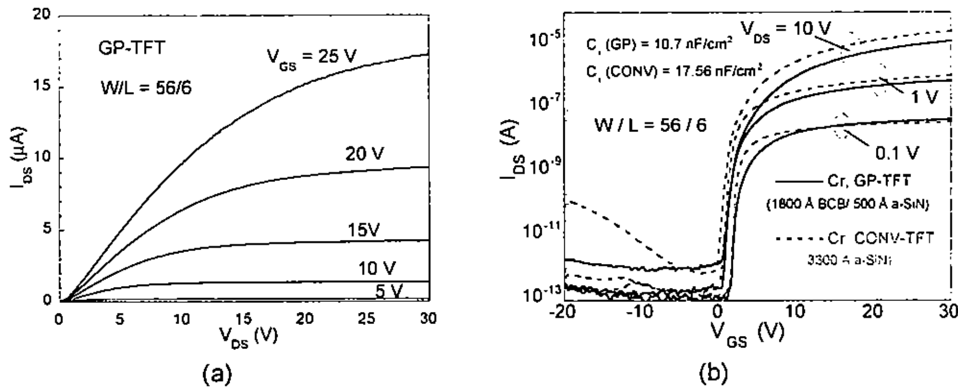

FIGURE 3.29 (a) Output characteristics of the GP-a-Si:H TFT. (b) Transfer characteristics of the GP-TFT (solid lines) and the conventional TFT (dashed lines) at different V_{DS} voltages. (Adapted from Ref. 52.)

maximum density of interface states (N_{ss}^{max}) is about 4 × 10^{11} $cm^{-2}eV^{-1}$ [27]. To compare the GP-TFT electrical performance with that of conventional devices, Cr-gate TFTs having the same PECVD materials, except a 3300-Å-thick a-SiN_x:H layer (C_i = 1.8 × 10^{-8} F/cm^2), were fabricated. The *S*-value obtained for the conventional TFT at V_{DS} = 0.1 V is about 0.26 V/dec, which corresponds to N_{ss}^{max} ~ 3.8 × 10^{11} $cm^{-2}eV^{-1}$. The GP- and conventional TFTs have very similar N_{ss}^{max} values, indicating that the quality of the a-SiN_x:H/a-Si:H interface is similar in both devices. The field-effect mobility (μ_{FE}) and threshold voltage (V_T) of the GP-TFT in the linear regime are about 0.30 cm^2/V-s and 3.48 V, respectively, while in the saturation region they are about 0.90 cm^2/V-s and 5.96 V, respectively. The μ_{FE} and the V_T values for the conventional TFT are about 0.25 cm^2/V-s and 1.93 V in the linear region and 0.95 cm^2/V-s and 2.56 V in the saturation region, respectively. The higher V_T found for the GP-TFT is associated with its smaller gate insulator capacitance: Normalized threshold voltage values $V_T \times C_i$ of GP- and conventional TFTs are comparable. The BCB thickness had no effect on the TFT field-effect mobility and normalized threshold voltage, which can further confirm that the density-of-states of the a-Si:H layer and a-Si:H/a-SiN_x:H interface are not modified by the BCB film. However, a thicker BCB film resulted in a lower TFT drain current and a higher threshold voltage because of a reduction of the gate insulator capacitance. We should also note that a significant electrical instability of this type of device was observed [60], which can present a potential challenge for long-term operation. Electrical instability issues are discussed in Section 3.5.

3.4.3 Buried-Busline Hydrogenated Amorphous Silicon Thin-Film Transistor

To avoid the reduction of the TFT drain current and the increase in threshold voltage associated with gate planarization technology as mentioned earlier, a new device, named the buried-busline (BBL) structure, has been developed for large-area and high-resolution AMLCDs [60].

3.4.3.1 Buried-Busline Device Structure and Fabrication Process

A schematic cross section of the BBL structure is shown in Figure 3.30. In comparison with the conventional a-Si:H TFT busline structure, one additional photolithography step is needed in the BBL structure, to define the buried gate buslines.

First, a 4500-Å-thick Cr film (ρ_g = 3 × 10^{-5} Ω-cm) was deposited on a Corning 7059 glass substrate via rf sputtering. After patterning the Cr BBLs, a low-dielectric-constant planarization layer, benzocyclobutene (BCB; $\varepsilon_r \cong 2.4$), was spin-coated directly over the BBLs. Then the Cr/BCB layers were cured in

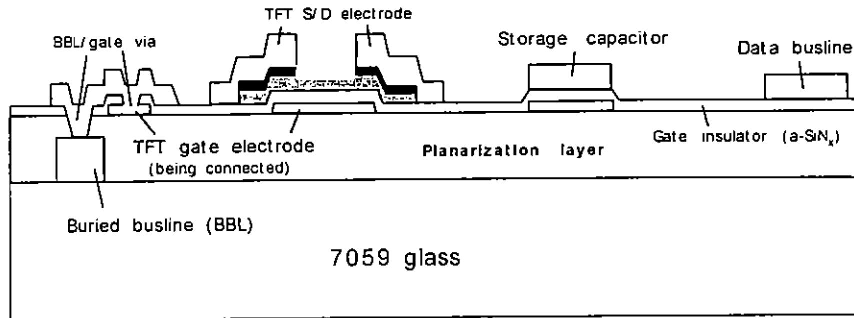

FIGURE 3.30 Schematic drawing of the BBL a-Si:H TFT structure. From [60].

a N_2 convection oven at 250°C for 1 hr. Following the BCB curing, a thin (700 Å) Cr layer was sputtered and patterned (TFT gate electrodes) over the BCB layer. Then amorphous silicon nitride, intrinsic and P-doped (n^+) a-Si:H films, having a thickness of about 2000, 2000, and 600 Å, respectively, were deposited via PECVD. After the active island definition, the BBL/gate via holes were opened through a-SiN_x:H and BCB layers by reactive-ionetch (RIE) using CF_4/O_2 gas mixture. Mo was used for the TFT source/drain metal contacts and BBL/gate via hole interconnects. Finally, the TFT back-channel etch was carried out by RIE using CF_4 gas.

Figure 3.31a shows the SEM picture of a TFT-pixel array incorporating the BBL structure. In this structure, to reduce the busline crossover capacitance,

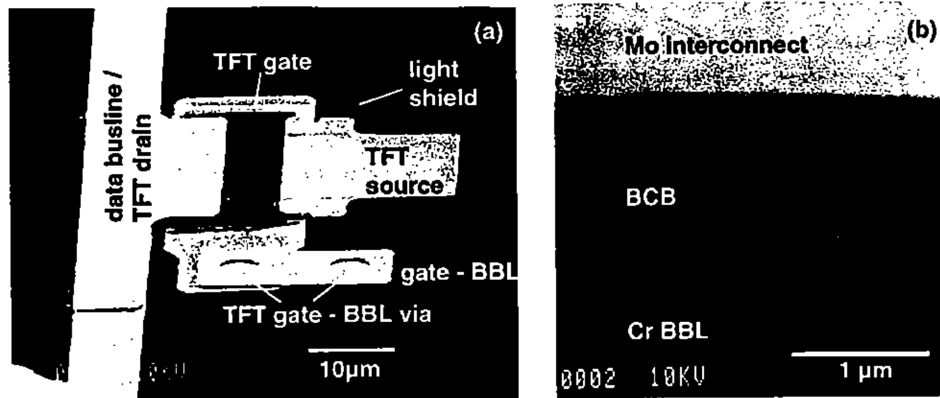

FIGURE 3.31 (a) SEM picture of the BBL-TFT structure; (b) cross-sectional SEM picture of the via hole over the gate BBL. (From Ref. 60.)

the gate busline (gate BBL) of the pixel arrays, which is connected to the TFT gate electrode, is buried by the BCB planarization layer. Figure 3.31b shows a cross section of the via hole over the BBL. It is clear from this figure that a very good conformal step coverage of the Mo interconnect over the BBL via hole has been achieved. This property ensures the absence of open circuits between the TFT gate electrodes and the BBLs. Also, in this structure the crossover defects (e.g., shorts and open circuits) between gate BBLs and data buslines can be prevented, since the gate BBL has been isolated from the source/drain metal layer.

3.4.3.2 Buried-Busline Device Electrical Performance

Figure 3.32a shows the transfer characteristics of the BBL (in solid lines) and the conventional- (CONV-; in dashed lines) a-Si:H TFTs for different source–drain voltages (0.1, 1, and 10 V). For the conventional TFT, a-Si:H and n^+a-Si:H layers of comparable thickness have been used; but the Cr gate electrode and a-SiN_x:H gate insulator are 1500 and 3000 Å thick, respectively. This figure indicates that the BBL-TFT has a higher ON-current than the conventional TFT, due to its

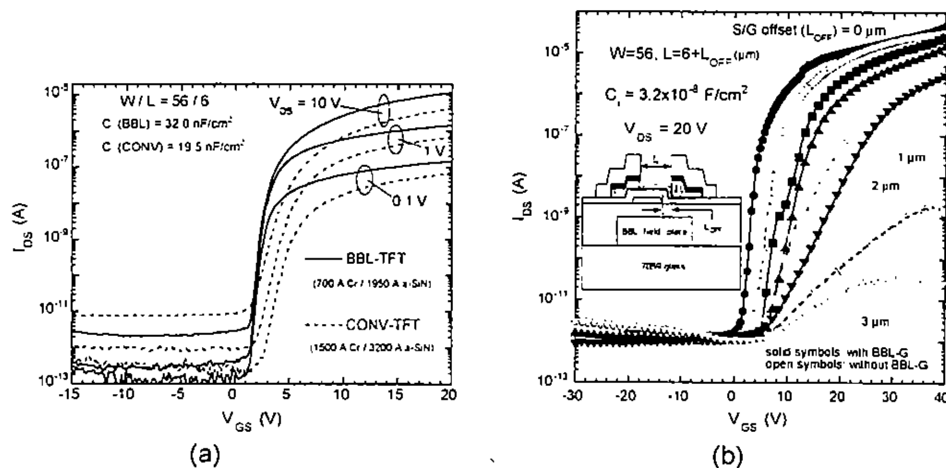

FIGURE 3.32 (a) Transfer characteristics of the BBL (solid) and the conventional (CONV-) (dashed) a-Si:H TFTs for different V_{DS} voltages. (b) Transfer characteristics of the BBL a-Si:H TFTs with source/drain gate offset ranging from 0 to 3 μm. The inset shows the cross section of the BBL TFT with source/drain gate offset. (From Ref. 60.)

larger gate insulator capacitance per unit area (C_i). In addition, the BBL-TFT has a smaller OFF-leakage current, which can be attributed to a better step coverage of the a-SiN_x:H layer over a thin (700 Å) Cr gate electrode used in the BBL structure. The subthreshold swing (S) of the BBL-TFT is about 0.31 V/dec, which corresponds to a maximum density of interface states of about 8×10^{11} $cm^{-2}eV^{-1}$. The BBL-TFT field-effect mobility in the linear regime ($L = 6$ μm) is about 0.33 cm^2/V-s, similar to the value obtained for the conventional TFT (0.34 cm^2/V-s). Normalized threshold voltages are also similar, but, as expected because of its thinner gate insulator, the BBL-TFT has a lower threshold voltage (2.57 V) than the conventional a-Si:H TFT (4.07 V).

The BBL structure can also be used as a light-shield or field-plate electrode underneath the TFT gate electrode. This light-shield electrode can reduce the photoinduced leakage current in the TFT channel region associated with multiple reflection due to the backlight illumination. The other applications of the BBL structure are a low-feed-through-voltage TFT and a high-voltage TFT when the BBL is used as a field-plate placed underneath the normal TFT gate electrode (both electrodes are connected) [61,62]. In the conventional a-Si:H TFT structure, because of the nonnegligible series resistance, certain source/drain-to-gate overlap ($\Delta L_{S/D\text{-}G}$) is needed to increase the TFT ON-current level [19,36]. In contrast, with the BBL field plate, the current levels are very similar for the TFTs having different $\Delta L_{S/D\text{-}G}$ ranging from 0 to 3 μm [52]. This can be attributed to the formation of the extended electron channel (in the a-Si:H layer adjacent to the a-SiN_x:H layer) over the BBL field plate (outside the TFT gate electrode); i.e., the effective $\Delta L_{S/D\text{-}G}$ has been increased when the BBL field plate is added to the conventional a-Si:H TFT. The formation of such a conductive channel due to the electron accumulation by the BBL field plate (BBL-G) can thus maintain a high TFT ON-current. This is a very important foundation for AMLCDs. The direct consequence of this discovery is that the TFT ON-current level is not reduced when the gate-to-source/drain overlap capacitance ($C_{gs} \propto \Delta L_{S/D\text{-}G}$) is reduced. Hence, smaller feed-through voltages are produced in display operation due to smaller C_{gs} values.

Finally, the BBL can be applied to a high-voltage a-Si:H TFTs [62]. In conventional high-voltage a-Si:H TFTs, an offset between the TFT gate and drain/source electrodes is needed [63]. This gate offset can increase the TFT operating voltage range, but at the same time it reduces the TFT ON-current because of a large increase in the channel resistance along the nonoverlap gate–source/drain regions. As shown in Figure 32b, BBL-TFTs have much higher I_{DS} currents than conventional high-voltage TFTs without the BBL field plate. This is clearly visible for a large gate offset (L_{OFF}). This type of high-voltage TFT structure is very attractive for LCDs requiring high-voltage switching devices, such as active-matrix reflective cholesteric LCDs [64].

3.4.4 Fully Self-Aligned Hydrogenated Amorphous Silicon Thin-Film Transistor

In the past, several researchers have introduced inverted-staggered self-aligned a-Si:H TFT structures to reduce the capacitive component of the TFT gate delay [35,65–68]. In all structures, the source/drain electrodes were aligned with the gate electrode by a back-substrate exposure technique [66], which simplifies the TFT fabrication. However, the intrinsic a-Si:H layer needs to be very thin to allow the UV light to pass through the a-Si:H layer for patterning the source/drain electrodes. The gate electrode should also be very thin in order to reduce the step coverage, resulting in an increased resistive component of the gate delay. A fully self-aligned (FSA) BCE Al-gate a-Si:H TFT has been developed [69] to reduce the gate line resistivity by using Al metallurgy.

3.4.4.1 Fully Self-Aligned Back-Channel-Etched Thin-Film Transistor Structure

This FSA BCE Al-gate a-Si:H TFT [69] requires only two masks, incorporating anodic aluminum oxidation and back-substrate exposure techniques. First, an Al-gate electrode was defined on a Corning 1713 glass substrate, followed by anodic oxidation (mask #1) [70]. Then the n^+ a-Si:H/a-Si:H/a-SiN_x:H layers were deposited via PECVD in one pump-down at a substrate temperature of 300°C. A successive deposition of different layers in one pump-down is essential for high-performance, stable TFTs. Next, a positive photoresist (Microposit 1827) was coated on the top and illuminated by UV light from the glass substrate side (back-substrate exposure). The a-Si:H and n^+ a-Si:H layers should be very thin to allow exposure of the photoresist, since a-Si:H-layer light absorption is film-thickness dependent. The UV wavelength that can be used for back-exposure ranges from 365 to 405 nm. In this experiment, the transmittance of the UV light was about 90 and 100% for Corning 1713 glass substrate and a-SiN_x:H film, respectively. However, the UV light transmittance decreased drastically for thick a-Si:H layers. Consequently, this FSA a-Si:H TFT process can work only for a-Si:H layers thinner than 1000 Å. To achieve good step coverage over the gate electrode, the Al sidewall profile was tapered during the patterning in a wet enchant solution of a mixture of phosphoric acid, nitric acid, acetic acid, and DI water. Next, a chromium (Cr) metal layer was deposited at room temperature via DC magnetron sputtering. After the liftoff process, the TFT channel area over the gate was opened, with the n^+ a-Si:H layer uncovered. The liftoff was done in hot liquid under ultrasonic agitation. The channel etch-back of n^+ a-Si:H was carried out via RIE using O_2 and CCl_2F_2 chemistry. Then the source and drain electrodes were patterned with photomask (mask #2). The Cr etching was done with a mixture of acetic acid and ceric ammonium nitrate. RIE etching of the

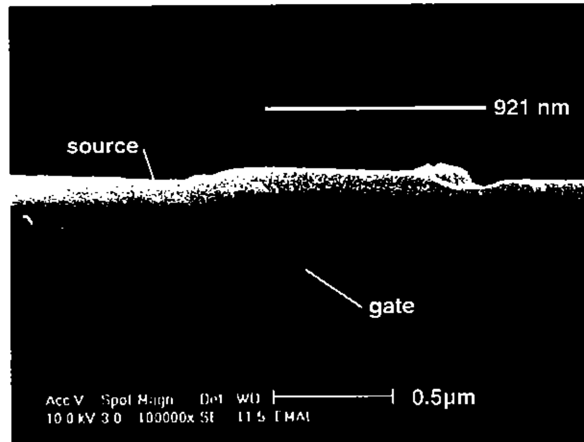

FIGURE 3.33 SEM picture of FSA BCE Al-gate a-Si:H TFT. The overlap between gate and source/drain electrodes is 921 nm. (From Ref. 69, with permission from Society for Information Display.)

n^+ a-Si:H anda-Si:H layers followed the wet etching of the source/drain area to avoid additional photomask for active-island definition. The typical thicknesses of each layer were 700 Å for Al, 3000 Å for a-SiN_x:H, 220 Å for a-Si:H, 100 Å for n^+ a-Si:H, and 1500 Å for Cr.

A SEM photograph of a self-aligned BCE a-Si:H TFT with a gate length of 7 μm is shown in Figure 3.33. The overlap between the gate and the source–drain electrodes is about 1 μm and was found to be uniform. This source/drain–gate overlap is attributed to the UV-light diffraction effect during the back-exposure. Changing the exposure and development times controls the overlap length, which ranges from 0.4 to 1 μm. This value is much smaller than the typical overlap of conventional a-Si:H TFT (~3 μm), which decreases parasitic capacitance and *RC* delay associated with the scan buslines.

3.4.4.2 Fully Self-Aligned Back-Channel-Etched Thin-Film Transistor Electrical Performance

Figure 3.34 shows the output and transfer characteristics of a FSA TFT with $W/L = 56/7$. The TFT field-effect mobility and threshold voltage in the saturation regime are 0.58 cm^2/Vs and 14.56 V, respectively. The corresponding normalized threshold voltage is about 3×10^{-7} C/cm^{-2}. The TFT OFF-current is 2.4×10^{-13} and the ON-OFF-current ratio is about 2×10^7. The subthreshold swing is

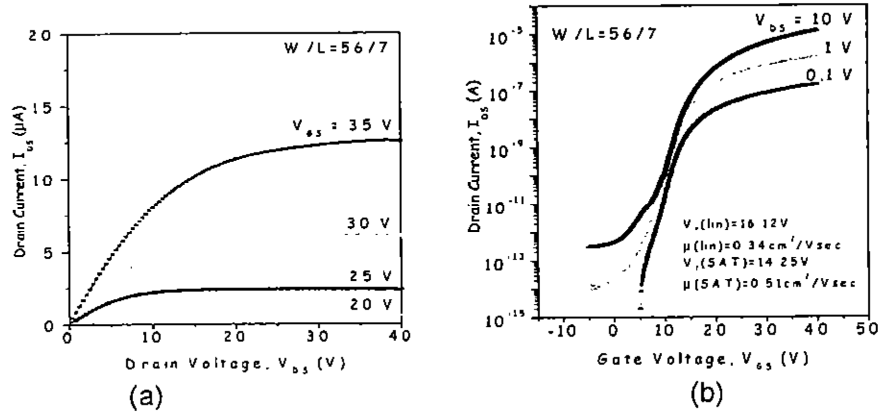

Figure 3.34 (a) Output and (b) transfer characteristics of an FSA BCE Al-gate a-Si:H TFT. (From Ref. 69, with permission from Society for Information Display.)

about 1.5 V/dec, corresponding to a maximum density-of-states at the amorphous semiconductor/gate insulator interface of about $3 \times 10^{12} cm^{-2} eV^{-1}$. The rather high normalized threshold voltage and subthreshold swing of this FSA a-Si:H TFT may result from a high density-of-states present in the thin a-Si:H layer [26]. On the other hand, a thin a-Si:H layer yields low source/drain access resistances. Indeed, the TFT field-effect mobility and threshold voltage showed little channel length dependence for channel lengths above 7 μm, which can be attributed to reduced source and drain access resistances [26]. The lack of current crowding in our FSA Al-gate a-Si:H TFT output characteristics [69] also supports the idea of small source/drain access resistances.

3.4.5 Top-Gate Hydrogenated Amorphous Silicon Thin-Film Transistors

3.4.5.1 Device Structure and Fabrication Process

So far, most display manufacturers have adopted bottom-gate a-Si:H TFTs in AM-LCDs [2]. However, the top-gate TFT structure can be very attractive, because of, among other things:

1. The possible use of a very thin a-Si:H layer, which can reduce the light-induced TFT leakage current [2].
2. The gate lines, being deposited at the top of gate insulator, can be very thick (no step coverage concern over the gate lines as it is the case for

bottom-gate TFTs) to reduce the gate-line *RC* delay in a large-area high-resolution AMLCDs [71].

3. A smaller number of photomask steps, in comparison with some bottom-gate a-Si:H TFTs, can lower the AMLCD production cost [72].
4. The possible modification of the conduction channel region could improve the a-Si:H TFT performance.
5. The compatibility with poly-Si TFTs that are used to fully integrate the AMLCDs.

The top-gate TFT structure was used as early as 1984 [73] when CNET (Centre National d'Études des Télécommunications, France) fabricated the "NS2S" structure (normal staggered, two photomask steps). The biggest advantage of this structure was its very simple process, resulting in a very low fabrication cost. However, the NS2S structure was not adopted by display manufacturers because of its poorer electrical performance in comparison with the standard bottom-gate TFT structures [2].

Today, the electrical performance of all TFTs are comparable, mostly because of the improved quality of the interface between a-Si:H and a-SiN_x:H. Also, the quality of the source and drain contacts has been improved by using either the selective deposition of *P*-doped ($n+$) a-Si:H layers [74] or the phosphine treatment (*P*-treatment) of the ITO contacts [75]. Both methods will ensure a high-quality ohmic source and drain contacts and a reduced number of photomask steps.

Top-gate TFTs have also been used in AMLCDs, initially [76] by the Hosiden Corp. and later by the Hosiden and Philip Display (HAPD) Corp. A top view and a cross section of a top-gate a-Si:H TFT are shown in Figure 3.35. In this

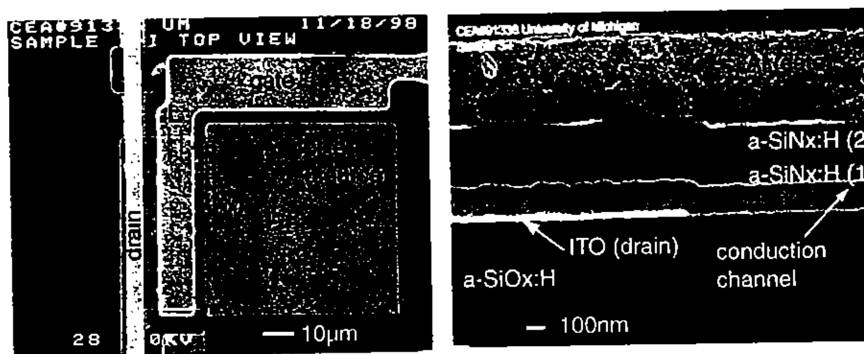

FIGURE 3.35 Top view and cross section of a top-gate a-Si:H TFT. (From Ref. 26.)

structure, a first gate insulator layer is deposited just after the a-Si:H and during the same deposition process. The active island (a-Si:H and a-SiN_x:H(1) layers) is then patterned before the deposition of the second insulator layer (a-SiN_x:H(2)). The number of mask steps required to produce this TFT is 4, which is comparable to or less than the number needed for the fabrication of typical bottom-gate TFT structures (4 and 5, for the back-channel-etched and the tri-layer structures, respectively). More precisely, the fabrication sequence for these top-gate TFTs is the following: first, a metal electrode (light shield) is deposited and patterned on glass substrates, and then it is covered with silicon oxide (a-SiO_x:H). Next, an indium–tin oxide (ITO) layer is deposited and patterned to form source and drain electrodes, and selective phosphorus treatment of the ITO-patterned electrodes is employed to achieve ohmic source/drain contacts [77]. Then an intrinsic a-Si:H/a-SiN_x:H bi-layer and a second a-SiN_x:H gate insulator are deposited by PECVD at 250°C. Finally, aluminum is deposited and patterned as the TFT gate electrode.

The phosphorus treatment of the source and drain electrodes is a critical step in the TFT fabrication, for it ensures the ohmic contacts that are necessary to achieve high-performance devices. Indeed, TFTs fabricated using a similar process but without the phosphorus treatment exhibited poor electrical performance and severe current crowding associated with high source and drain series resistances. Secondary ion mass spectrometry (SIMS) analysis of treated ITO electrodes has shown the high selectivity of the phosphine treatment. After treatment, the concentration of phosphorus atoms on the ITO electrodes is more than a decade higher than the concentration of phosphorus atoms on the substrate outside of the ITO electrodes. In addition, X-ray photoelectron spectroscopy (XPS) was used to show that, following the phosphorus treatment of ITO surface, an InP layer is formed at the ITO-treated surface. These results are consistent with other analyses performed on similar samples [75].

The electrical properties and the quality of the a-SiN_x:H(1) layer are critical for the TFT electrical performance. Indeed, a significant improvement in device performance, especially the apparent field-effect mobility, has been obtained by using the aminosilane regime for the deposition of the a-SiN_x:H(1) layer [78]. The quality of the interface between the a-Si:H and the a-SiN_x:H layers is also important for the device electrical performance. High-performance top-gate TFTs have been fabricated by using a nitridation process for the a-Si:H surface before the deposition of a-SiN_x:H gate insulator [79]. Output and transfer characteristics curves for a top-gate TFT are shown in Figure 3.36.

3.4.5.2 Electrical Performance

Top-gate a-Si:H TFTs with electrical performance similar to bottom-gate TFTs have been fabricated. For an 8-μm-long TFT ($W = 50$ μm) with a-Si:H and a-

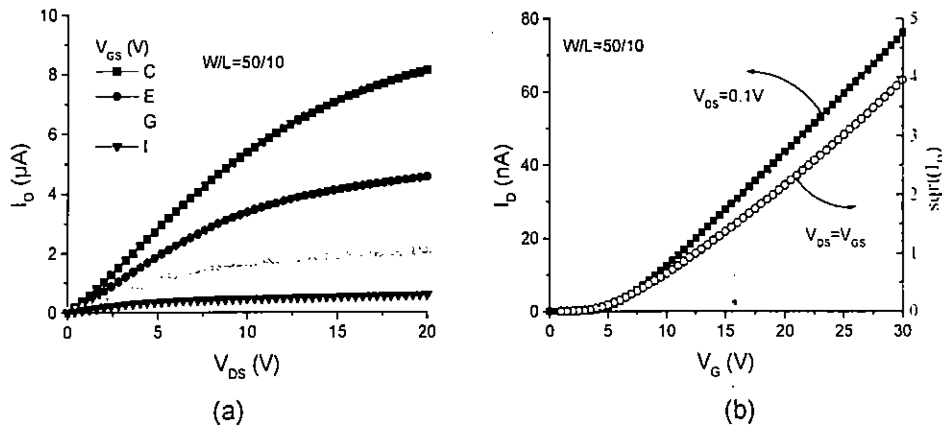

FIGURE 3.36 (a) Output and (b) transfer characteristic of top-gate a-Si:H TFT.

SiN_x:H thicknesses of 1350 and 2600 Å, respectively, the following performance was obtained:

- Field-effect mobility of 0.52 and 0.57 cm^2/V-s in the linear and saturation regimes, respectively
- Threshold voltage of 2.4 and 2.2 V in the linear and saturation regimes, respectively, corresponding to a normalized threshold voltage $V_T \times C_{ins} = 5.5 \times 10^{-8}$ and 5.1×10^{-8} C/cm^2 in the linear and saturation regimes, respectively
- Subthreshold slope of 0.57 V/dec (in the linear regime). corresponding to a maximum density of states at the amorphous semiconductor/gate insulator interface of about 10^{12} $eV^{-1}cm^{-2}$ [27]

The electrical performance of these top-gate a-Si:H TFTs are comparable to the typical electrical performance observed for bottom-gate a-Si:H TFTs, which shows that the general belief that top-gate a-Si:H TFTs have a worse electrical performance than bottom-gate a-Si:H TFTs is not always valid [2,80].

3.5 ELECTRICAL INSTABILITIES IN HYDROGENATED AMORPHOUS SILICON THIN-FILM TRANSISTORS

It has now been well established that a-Si:H/a-SiN_x:H TFTs are not as stable as their crystalline MOSFET counterparts, but instead exhibit a shift in threshold voltage as a result of prolonged application of gate bias. Experimentally it has been established that this threshold voltage shift is a function of a number of

factors, including the magnitude, polarity, and duty cycle of the applied gate bias stress, the temperature at which the TFT is stressed, and the total stress time [81]. Underlying these observations is the understanding that these instabilities reflect the electronic quality of the PECVD a-Si:H and a-SiN_x:H films as well as the interface between them, since it is known that threshold instability can be minimized by careful control of process conditions such as deposition rate, gas flow ratio, and substrate temperature, which are known to control hydrogen content and bonding in the films.

The instability in a-Si:H TFTs has generally been attributed to one of two mechanisms: charge injection and subsequent trapping in the a-SiN_x:H gate insulator, or a bias-induced increase in silicon dangling-bond states in the a-Si:H. Often both mechanisms are invoked simultaneously to explain a range of experimental results, and either may dominate, depending on sample preparation conditions. The rationale behind the model for increased density of deep states within the a-Si:H has its origins in experiments showing degradation of TFT characteristics after prolonged illumination [82], and thus a connection to the well-known creation of metastable dangling-bond states observed in the Staebler–Wronski effect [83]. Hepburn et al. studied charge trapping and release from a-Si:H/a-SiN_x:H/n+ c-Si samples using alternating combinations of gate stress, photoinduced discharge, and thermal annealing [84]. They fit their photoinduced decay data using a Gaussian trap model with an energy depth of 0.85 eV and an attempt-to-escape frequency of 10^{12} Hz, but found a second activation energy of 1.5 eV in their annealing data. The thermal activation energy was attributed to dangling-bond states similar to those responsible for the Staebler–Wronski effect, since these were known to have a 1.5-eV activation energy [85]. As for the photodecay results, since charge release was found to drop to zero for illumination at sub-band-gap energies, internal photoemission was effectively ruled out. These observations were explained as resulting from the neutralization of the residual deep-trapped charge by the generation and redistribution of photoinduced carriers, rather than from direct release from trapping centers. It was postulated that population of the a-Si:H tail states induced by optical illumination could result in a silicon atom having an unstable configuration; a similar mechanism was suggested by Street to occur as a result of phosphorus doping [86]. The unstable situation is resolved by the breaking of weak Si–Si bonds and the formation of dangling-bond defects:

$$2Si_4^0 + e \rightarrow Si_3^- + Si_3^0 \tag{3.44}$$

During the late 1980s, investigations were performed to elucidate whether deep-trap creation in the a-Si:H or charge injection into the a-SiN_x:H gate insulator played the primary role in TFT instability [87]. The use of an ambipolar transistor proved to be an excellent investigative tool for this purpose. An ambipolar a-Si:H TFT is one in which both electron and hole currents flow (albeit not equally, due to the large difference in electron and hole mobility), and it is produced

simply by dropping the $n+$ a-Si:H source and drain contact layers from the fabrication process. In order to have sufficiently large drain currents and to avoid undesirable contact resistance effects, these devices are usually physically quite large. Their utility lies in the fact that characteristic curves are produced for both negative and positive gate bias in the same device. If charge injection in the gate insulator is responsible for the TFT electrical instability, we expect a rigid shift of both the electron and hole conduction curves along the gate voltage axis *in the same direction*. On the other hand, if the density of deep-gap states is modified in the a-Si:H and the Fermi level moves through these states in establishing the conduction channel accumulation layer, then we expect the electron and hole current-voltage curves to shift in *opposite directions*. The band-bending diagrams showing deep-gap states filling under accumulation and inversion for this scenario are illustrated in Figure 3.37.

Three sets of transfer characteristics for an ambipolar TFT are shown in Figure 3.38 corresponding to the following sequential experimental conditions: after annealing at 180°C (no stress), after +25 V stress for 4 hours, and again after −25 V stress. In this case, the transfer characteristics for electron and hole currents corresponding to the positive stress condition move in opposite directions, indicating an increase in deep-gap states in the a-Si:H. The curves shift in the *same* direction, however, for the negative gate stress condition, indicating a net positive charge in the amorphous silicon nitride layer and little further defect creation. Interestingly, when the same experiment was repeated, but with a large positive bias voltage of +70 V following the initial +25 V stress, the final set of curves both shifted to the right by nearly equal amounts, indicating that charge

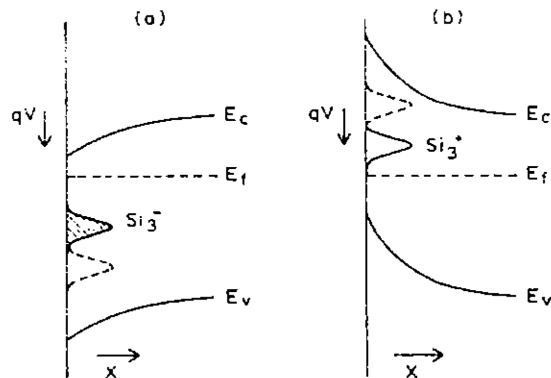

Figure 3.37 Band bending in a-Si:H under accumulation (a) and inversion (b). The created dangling bonds are negatively charged under positive bias and positively charged under negative bias. (From Ref. 87.)

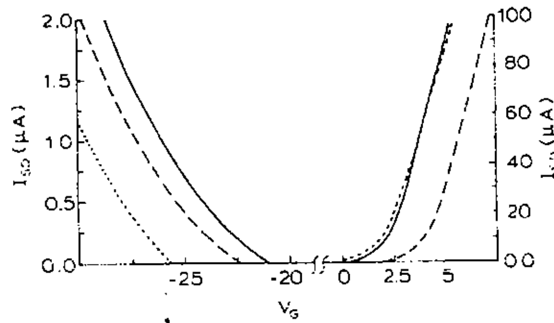

FIGURE 3.38 Ambipolar transfer characteristics corresponding to the following conditions: solid lines—after 180°C anneal; dashed lines—after +25-V bias stress for 4 hours; dotted lines—after −25-V bias stress for an additional 4 hours. (From Ref. 87.)

injection into the a-SiN_x:H gate insulator becomes dominant at high positive gate stress. Clearly both a-Si:H deep-gap-state creation and charge injection were seen to play roles in the materials chosen for this study.

On some other ambipolar devices, the results were slightly different [88]. Figure 3.39 shows transfer characteristics of ambipolar bottom-gate TFTs before and after positive and negative stress. Positive stress results in a shift of the

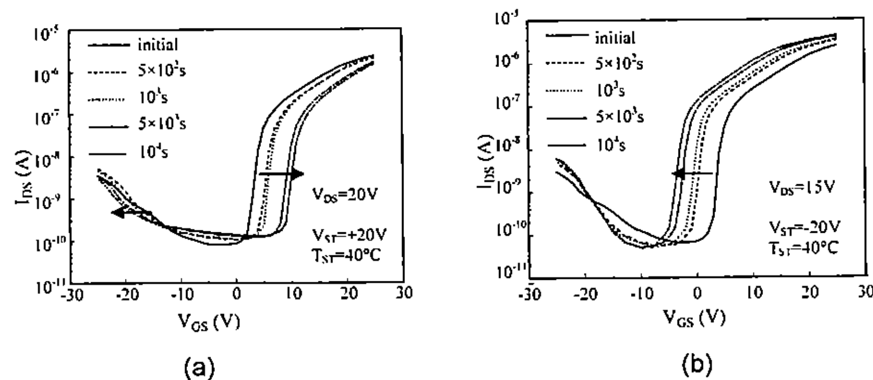

FIGURE 3.39 Evolution of ambipolar a-Si:H TFTs transfer characteristics under (a) positive and (b) negative steady-state gate bias-temperature-stress. Stress and measurements were performed at 40°C. (From Ref. 88)

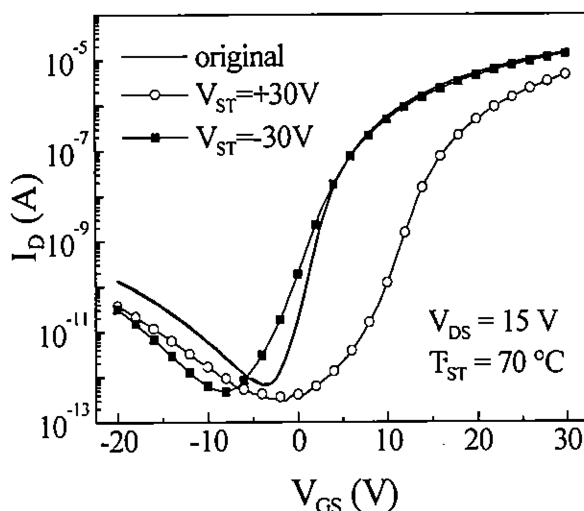

FIGURE 3.40 Evolution of conventional top-gate a-Si:H TFTs transfer characteristics after positive and negative steady-state gate bias-temperature-stress. Stress and measurements were performed at 70°C.

electron branch towards positive gate voltages while the hole conduction branch shifted towards positive voltages for short stress times, then towards negative voltages. This suggests mostly an increase of the density of deep-gap states in a-Si:H near the a-Si:H/a-SiN_x:H interface and a possible charge trapping in the gate insulator. The negative stress resulted in a shift of the electron conduction branch towards negative voltages and no significant shift of the hole branch. This corresponds to a decrease of deep-gap states in the band-gap region in combination with charge trapping in the a-SiN_x:H layer [88].

The simultaneous investigation of the electron and hole conduction branches has also been performed through measurements of conventional top-gate a-Si:H TFTs at high temperatures, as seen in Figure 3.40. Here, a positive stress results in electron and hole branches shifting towards positive and negative voltages, respectively, suggesting a creation of deep-gap states. Negative stress, on the other hand, results in almost no change of the electron branch and a shift of the hole branch towards negative voltages, which suggests that both defect creation and charge injection in the gate insulator occurred.

By the early 1990s, improvements in a-Si:H material quality and experiments with new structures and measurement techniques were suggesting that

although both instability mechanisms played roles, charge injection into the gate insulator was dominant. Gelatos and Kanicki stressed a-Si:H/a-SiN_x:H capacitors both positively and negatively, and used pulsed photocapacitance measurements to separate "fast" interface and/or a-Si:H bulk states from "slow" states within the gate insulator [89]. As in previous studies, they found that negative stress had no effect on a-Si:H bulk states but could lead to positive charge trapping in the gate insulator. It was determined that positive bias stress led to both a-Si:H gap-state creation as well as negative charge accumulation in the gate insulator but that no more than about one-third of the measured shift in the *CV* curves could be accounted for by a-Si:H bulk states measured by photocapacitance. In other words, charge injection into the insulator was the dominant factor.

A number of possible electron injection mechanisms leading to TFT instability were proposed by Powell [90], including Fowler–Nordheim injection, trap-assisted injection, and constant-energy tunneling from the a-Si:H conduction band, among others. These are illustrated in Figure 3.41. Building on results showing charge injection to be primarily responsible for TFT threshold shift,

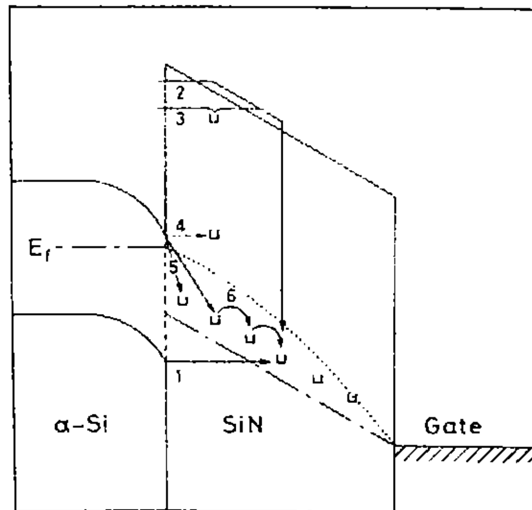

Figure 3.41 Charge injection mechanisms from a-Si into a-SiN_x:H gate insulator: 1—direct tunneling from the valence band; 2—Fowler–Nordheim injection; 3—trap-assisted injection; 4—constant-energy tunneling from conduction band; 5—tunneling from conduction band to insulator Fermi level (phonon assisted or via surface states); 6—hopping at the Fermi level. (From Ref. 90.)

Libsch and Kanicki found they could adequately model all their bias-temperature-stress (BTS) data, regardless of the magnitude of the stress bias, its polarity, or the temperature at which the stress was applied, using the following stretched-exponential equation [88,91]:

$$|\Delta V_T| = |\Delta V_o| \left\{ 1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta} \right] \right\} \tag{3.45}$$

where $\tau = \tau_o \exp(E_\tau/kT)$ represents the characteristic trapping time of carriers, and $|\Delta V_o|$ is approximately the voltage drop across the insulator, given by $\sim |V_G - V_{To}|$, where V_{To} is the initial threshold voltage. In this model, the thermal activation is given by $E_a = E_\tau \beta$, with β being the stretched-exponential exponent; $E_\tau = E_a/\beta$ is interpreted as the average effective energy barrier that carriers in the a-Si:H channel need to overcome before they can enter the insulator, and τ_o is the thermal prefactor for emission over the barrier. For short stress times, lower-stress fields, or low stress temperatures, carriers hop or inject directly into lower-energy states located at the a-Si:H/a-SiN_x:H interface and into a transitional layer in the nitride close to the interface. At longer stress times, higher-stress fields, and higher temperatures, a larger fraction of states in the insulator near the interface are filled, leading to an increased probability of emission from these states. The model proposes that the amorphous structure of the a-SiN_x:H gate insulator will lend itself to an appreciable number of band-tail states, which act as transport states for the emitted lower-energy trapped charge, and this distribution of multiple trap levels yields the time-dependent power law in the argument of the exponent of Eq. (3.45). Threshold voltage shift data at a gate bias of +25 V for temperatures ranging from 22°C to 125°C are fitted by the model in Figure 3.42.

Further modeling of the bias-temperature stress-induced threshold voltage shift has been proposed, unifying the effect of the stress time and temperature [92]. It is based upon the thermalization energy $E = kT_{ST} \ln(\nu t_{ST})$, where k is the Boltzmann constant and ν is the attempt-to-escape frequency, taken in [92] as 10^{10} Hz for all stress temperatures. The authors have shown that the ΔV_T-E curves overlap perfectly for all stress temperatures, and have identified a characteristic energy (corresponding to the inflexion point of the ΔV_T-E curves) that is assumed to be associated with the most likely defect creation energy barrier. Similar experiments performed on a series of other devices, having different structures such as the ones discussed previously in this chapter required adjustment of the value of V and resulted in ΔV_T-E curves still exhibiting very significant temperature dependence, as shown in Figure 3.43a [93]. However, by using a semi-empirical method based on a many-body approach proposed by the authors, it was possible to identify a characteristic time t_{peak} from the ΔV_T-Log(t_{ST}) curves and to establish normalized curves ΔV_T versus $t^*_{ST} = t_{ST}/t_{peak}$ that were identical for all devices measured, as shown in Figure 3.43b.

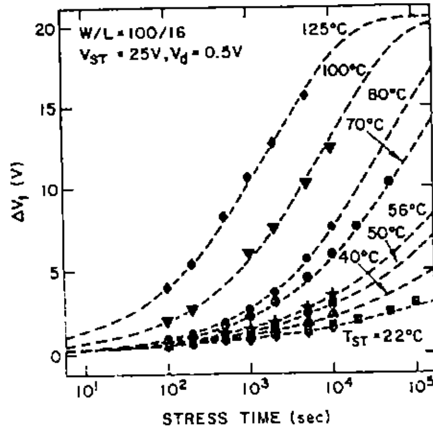

FIGURE 3.42 Threshold voltage shift ΔV_T versus time for a gate bias stress of +25V and for temperatures ranging from 22°C to 125°C. The symbols represent the data, and the dashed lines represent the fits to Eq. (3.45). (From Ref. 91.)

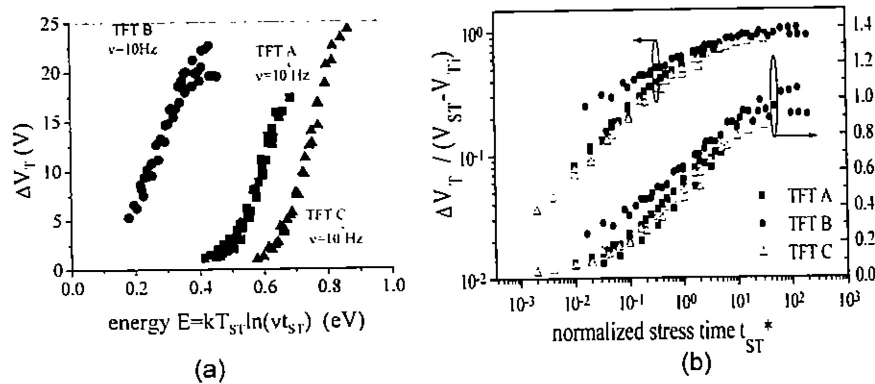

FIGURE 3.43 (a) Threshold voltage shift measured for different a-Si:H TFTs for a stress voltage of 30V and stress temperatures between 50 and 110°C as a function of the energy $E = kT_{ST}\ln(\nu t_{ST})$. The values of ν were determined to ensure, for each TFT, the best overlap of the ΔV_T-E curves for all stress temperatures. (b) Same data plotted under the form ΔV_T versus $t^*_{ST} = t_{ST}/t_{peak}$. (From Ref. 93.)

The success of all these models consists in their ability to ultimately predict future threshold shift behavior far out in time. However, all the models presented above address steady-state (DC) electrical stress, i.e. experiments during which the TFT gate voltage is constant. In AMLCDs, a-Si:H TFTs are under pulsed gate-bias addressing with a typical frequency of 60 Hz [94]. Therefore, from a practical point-of-view, to obtain a good estimation of the long-term reliability of a-Si:H TFTs in AMLCDs, it is necessary to understand the details of the electrical instability of a-Si:H TFTs under pulsed (AC) gate-bias stress conditions that are similar to a typical AMLCD addressing conditions. It has been pointed out that certain differences exist in ΔV_T between the steady-state and pulsed bias stresses [95,96]. Indeed, the investigation of the threshold voltage shift of bottom-gate back-channel-etched a-Si:H TFTs induced by pulsed BTS has shown that a significantly lower magnitude of threshold voltage shift was observed for negative AC BTS than for negative DC BTS [91]. The magnitude of the threshold voltage shift after negative AC BTS decreased with decreasing pulse width, as shown in Figure 3.44. A possible explanation is that the emptying of the traps and defect states that can occur during negative gate pulses occurs on a long time scale and

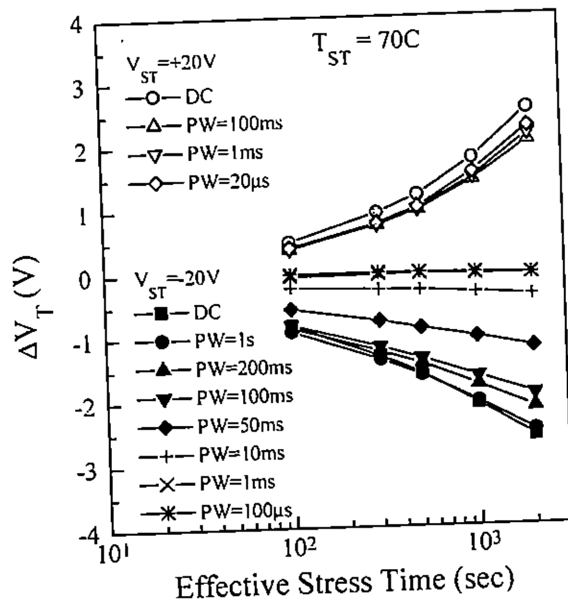

Figure 3.44 Threshold voltage shift versus effective stress time at different stress pulse-width for bottom gate a-Si:H TFTs under positive and negative BTS at ±20V, 70°C (from Ref. 88.)

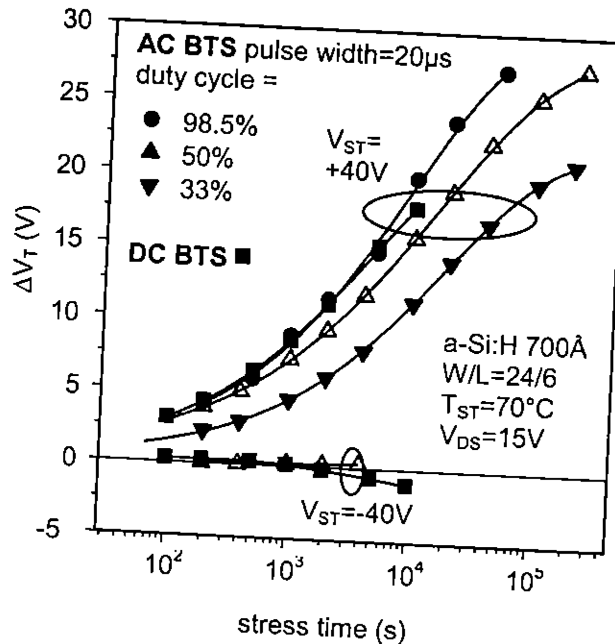

FIGURE 3.45 Threshold voltage shift for top-gate a-Si:H TFTs under BTS at 40V and 70°C, as a function of the effective stress time for different duty cycles (from Ref. 9).

is therefore affected by the duration of these gate pulses. Threshold voltage shift induced by positive AC BTS was only slightly lower than for DC BTS and pulse width-independent. It was reported previously that charge detrapping during pulsed operation could explain the smaller shifts induced by AC BTS [95]. In addition, relaxation of deep-gap defects during OFF-periods in the pulsed operation could also contribute to the threshold voltage shift differences [95].

For top-gate a-Si:H TFTs, observations have shown that the threshold voltage shift measured for positive AC BTS was lower than for positive DC BTS and decreased with decreasing duty cycle, as shown in Figure 3.45. On the other hand, negative DC and AC BTS experiments resulted in comparable, and very small, threshold voltage shifts [97]. The difference in the behaviors of these top- and bottom-gate a-Si:H TFTs has not been clearly explained, although it could be associated with the different nature of the a-Si:H/a-Si:N_x:H interface and/or the different characteristics of the materials used in both types of devices.

To address AMLCDs, the gate signals consist in a sequence of positive and negative pulses of different widths. It was established that the superposition

of positive and negative AC BTS will result in a net increase of the TFT threshold voltage. For AMLCD manufacturers, BTS modeling and threshold voltage shift calculation is a standard method of assuring adequate voltage margin over the lifetime of the active matrix. Margin in this sense is defined as the largest tolerable TFT threshold shift before current drive becomes insufficient to charge up a pixel during its scan time. By modeling accelerated threshold voltage shift results under higher temperature and/or different duty cycle and replotting the model under standard panel operational conditions, manufacturers can calculate whether their TFT process has adequate margin to meet their particular panel lifetime specification e.g. 60,000 hours (about 10 years). For the bottom gate TFTs above mentioned, a method of estimating ΔV_T of a-Si:H TFTs under pulsed bias-stress having both positive and negative gate-voltage cycles was proposed [88]. It resulted, for typical SXGA AMLCD driving conditions, in a TFT threshold voltage shift of about 3 V after about 10 years of operation at 70°C. The study of top-gate a-Si:H TFTs has indicated that threshold voltage shift would be larger than for the bottom-gate a-Si:H TFTs above mentioned but no final estimation has been proposed for the threshold voltage shift resulting from pulsed bias-stress representative of AMLCD driving scheme [97].

3.6 CONCLUSION

The results described in this chapter have addressed different aspects of a-Si:H TFT technology and may serve as a reference to the amorphous semiconductor community. In addition, the analysis and conclusions of this work and their significance could be a useful reference in the development of next-generation thin-film transistors based on organic semiconductors, which are discussed in subsequent chapters of this book.

ACKNOWLEDGMENTS

One of the authors (J.K.) would like to thank the following graduate students at the University of Michigan for their contributions to this chapter: Chun-Ying Chen, Chun-Sung Chiang, Joohan Kim, Jeffrey Lan, Tong Li, and Jeong-Yeop Nahm. The discoveries described here would not have been possible without their hard work and strong belief in their research.

The financial support of the University of Michigan Center for Display Technology and Manufacturing, Hosiden and Philips Display Corp., Dow Chemical Corp., Hitachi Corp., NEC Corp., and DARPA is also gratefully acknowledged.

We also wish to thank Dr. Paul Andry, from IBM Corp., for his help during the preparation of this manuscript.

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