Influence of gate dielectrics on the electrical properties of F8T2 polyfluorene thin-film transistors

James Swensen, Jerzy Kanicki, and Alan J. Heeger
Center for Polymers and Organic Solids, University of California at Santa Barbara, Santa Barbara, CA 93106-5090, USA

ABSTRACT

The electrical properties of polymeric thin film transisitors (P-TFTs) based on poly(9,9-dioctylfluorene-co-bithiophene) alternating copolymer (F8T2) have been studied. Device performance was compared for amorphous silicon nitride deposited by LPCVD and PECVD techniques, aluminum oxide deposited by sputtering, titanium oxide deposited by sputtering, and thermal silicon oxide gate dielectrics. A heavily n-type doped crystalline silicon wafer coated with the desired gate dielectric was used. Photolithographic patterning of source/drain electrodes directly on top of the F8T2 layer is also discussed. The main conclusion from this work is that traps within the F8T2 define the conduction process within the device.

Keywords: F8T2, polymer thin-film transistor, gate dielectrics, titanium oxide

1. INTRODUCTION

The gate dielectric layer is one of the critical materials in polymeric thin-film transistors (P-TFTs), since the electrical characteristics and the density of carriers in the conduction channel of the P-TFTs are controlled by the gate insulator capacitance. The drain current of the P-TFTs is linearly proportional to the capacitance of the dielectric material. Also the gate dielectric-polymer semiconductor interface can influence the measured mobility and therefore the P-TFT properties.

Various studies have been done on both high dielectric constant (ε) materials [1, 2, 3], and low-ε materials [4, 5, 6]. Usually these studies report on each material independently. Dimitrakopoulos et al. compared barium zirconate titonate (BZT) films, a high-ε material, to thermal SiO_2 [3]. They showed equivalent device performance and mobility at lower voltages due to the higher charge that was present across the higher dielectric constant material. The main purpose of this paper is to report on the effect that different gate dielectrics have on the electrical properties of P-TFTs.

Poly(9,9-dioctylfluorene-co-bithiophene) alternating co-polymer (F8T2) was used as the polymer semiconductor in the P-TFTs, as shown in Figure 1a. The following dielectrics were used as the gate insulator: titanium oxide (TiO_2), aluminum oxide (Al_2O_3), low pressure chemical vapor deposition amorphous silicon nitride (LPCVD α-Si_3N_4:H), plasma enhanced chemical vapor deposition amorphous silicon nitride (PECVD α-SiN_x:H), and thermal silicon oxide (SiO_2).

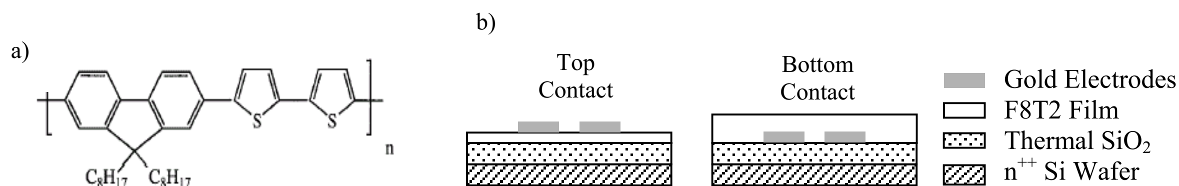

Figure 1. a) F8T2 chemical structure. b) Schematic showing top contact and bottom contact device geometries.

Various methods have been reported in the literature to pattern and deposit source/drain contacts. Photolithography and shadow masks were the first methods used. More recently techniques such as screen-printing[7,8], microcontact printing [9, 10], and inkjet printing [11, 12, 13] have been used. In nearly all of the above processes, the bottom source drain contact device configuration was used. Top and bottom source drain contact device geometries are illustrated in Figure 1.

Shadow mask deposition is the main process that has been used to define drain and source electrodes in the top source/drain contact device geometry. Channel lengths below 15 to 20 microns are difficult to achieve by shadow mask patterning. It is difficult to align the electrodes to patterned gates, which are necessary to reduce leakage current and enhance device performance in integrated circuits. In this paper we report on the patterning and deposition of top source/drain contacts using a photolithographic process directly on the F8T2 polymer semiconductor surface. To the best of our knowledge, this is the first time that this has been carried out. Devices with the resolution and size capabilities of photolithography have been obtained. Additionally, top contact devices patterned by photolithography can be aligned to an underlying patterned gate.

The top contact device configuration is desirable for a number of reasons. First, the polymer film should have better interface with the dielectric surface, and there is no step coverage over the electrodes as in the bottom source/drain contact structure. Second, in the top source/drain contact structure, a liquid crystal polymer can be processed and aligned on the clean and well defined dielectric surface, and then the contacts can be patterned over the F8T2. It is likely that greater mobility anisotropy can be obtained with this device structure. Third, recent work has shown that the top contact structure may in fact have better charge injection into the polymer semiconductor than bottom contact structure [14]. Additionally, processing techniques that have been developed for inorganic technology may be able to be applied to organic technology to enhance charge injection even further. One such example lies in the doping of the contact region of amorphous semiconductors before metal contacts are evaporated. This allows for better charge injection from the metal into the semiconductor, which in turn enhances device performance.

2. EXPERIMENTAL

Top Contact Device Fabrication

Five dielectrics films were chosen to be the gate insulator for the devices to be tested in this study: thermal SiO_2 ($\varepsilon = 3.7$), PECVD α-SiN_x:H ($\varepsilon = 7.2$), LPCVD α-Si_3N_4 ($\varepsilon = 7.4$), sputtered Al_2O_3 ($\varepsilon = 8.0$) obtained from Symmorphix (Santa Clara,CA), and sputtered TiO_2 ($\varepsilon = 38$) obtained from Symmorphix (Santa Clara,CA). All of the dielectrics films tested were deposited or grown on a heavily doped n^{++} Si wafer. The n^{++} Si served as the common gate in the thin-film transistor device structure used in this study. The capacitance of each dielectric was measured with a Keithley 590 Capacitance-Voltage Meter set at 100 MHz on Metal-Insulator-Metal (MIM) structures. In order to fabricate the MIM structure, photolithography was performed directly on the dielectric surface. The MIM structure is shown in Figure 2.

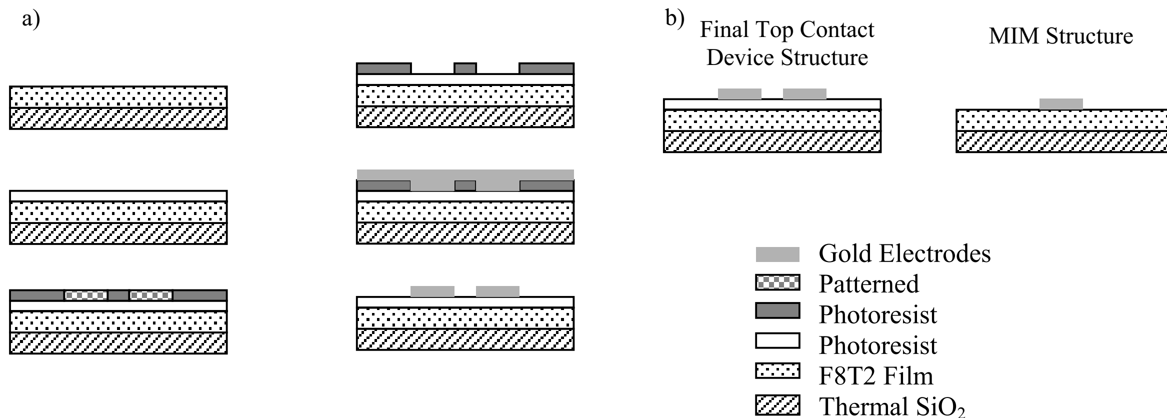

Figure 2. a) Schematic showing the device fabrication process for top source/drain contact devices. b) Schematic showing the final top source/drain contact device structure and a MIM device structure.

Figure 2 schematically depicts the fabrication process for the top source/drain contact P-TFT devices, which has been discussed in more detail in a previous work [15]. The process is as follows. Each dielectric sample was cleaned by sonication for 3 minutes in acetone, then rinsed with isopropanol and dried under a stream of $N_{2(g)}$. The substrates were then placed in an oven at ~100° C for five minutes to dry. The samples were removed from the oven and an F8T2 film was spin coated from a solution of 1% xylenes (98.5% purchased from Aldrich) onto the dielectric surface at 1500 rpm. The dielectric substrates were then placed in a vacuum oven, the chamber was evacuated to low pressure, and the devices were baked at ~115° C for 90 minutes. The film was measured to be ~140 nm thick by Dektak profilometry. Source drain contacts were defined via photolithography directly on top of the F8T2 surface. A 500 Å thick gold film was deposited at 2 $x10^{-6}$ T by thermal evaporation to form the contact areas.

Removing the un-patterned photoresist in acetone left the patterned gold electrodes in contact with the F8T2 surface as shown in Figure 2. These electrodes form well-defined top source/drain contacts with the resolution and alignment capabilities of photolithographic techniques. All of the devices tested for this study had a channel length of 10 µm and a channel width of 1000 µm. The devices were tested immediately after removing the photoresist and then again after sitting in air for three weeks using a Keithley 4200 Semiconductor Characterization System. The data presented here was the data set collected three weeks after device fabrication.

The top contact devices used in this study to fabricate the P-TFTs allowed us to study the electrical properties of devices where the semiconducting polymer was deposited directly on the native dielectric surface, without exposure to mono-layer treatments or photolithographic processes. We note that photolithographic patterning of top source/drain contacts could not be performed on surface of a poly(3-hexylthiophene) (P3HT) film. During the development of the patterned photoresist, the photoresist delaminated from the P3HT surface, and the P3HT also began to delaminate from the dielectric surface.

3. RESULTS AND DISCUSSION

The data sets reported on in this section are the transfer characteristics, drain to source current (I_{ds}) versus gate to source voltage (V_{gs}), in the saturation regime. As stated in the experimental section, the device geometry of the five dielectrics tested was the top source/drain contacts illustrated in Figure 2. Devices with bottom source/drain contacts were also fabricated with all the dielectrics studied. It was found that devices with TiO_2 and Al_2O_3 as the gate dielectric in the bottom source/drain contact geometry leaked too much to produce trustworthy results. The F8T2 film between the electrodes and the dielectric in the top source/drain contacts geometry served as a leakage barrier. As a result, functional TiO_2 and Al_2O_3 devices were tested with sufficiently low leakage current, meaning that I_{gs} was at least an order of magnitude lower than I_{ds}.

The dielectric constant (ε) of each gate insulator was calculated from the capacitance (C_o) measurements made on the metal-insulator-metal (MIM) structures (see Figure 2) and the dielectric thickness. $\varepsilon = C_i*d/\varepsilon_o$, where C_i (capacitance of the insulator) = C_o/A. A is the area of the MIM structure, d is the thickness of the insulator, and ε_o is the permittivity of free space in a vacuum. The results are shown in Table 1. The experiment was designed with C_i of the silicon nitrides and thermal silicon oxide to be equivalent so that the data collected on these devices would be directly comparable. For the TiO_2 and Al_2O_3, we used the dielectric thicknesses that were available. TiO_2 has a much larger dielectric constant than the other dielectrics and Al_2O_3 is thinner than the other dielectric films. As a result, the C_i across the gate insulator is larger for these two dielectrics than for the silicon nitrides or the thermal silicon oxide. Consequently, The P-TFTs made on TiO_2 and Al_2O_3 were expected to operate at lower voltages than the other dielectrics.

Dielectric	**C_i (F/cm^2)**	**Thickness (nm)**	**ε**
Thermal SiO_2	1.624 $x10^{-8}$	200	3.7
PECVD α –SiN_x:H	1.60 $x10^{-8}$	400	7.2
LPCVD α –Si_3N_4:H	1.64E $x10^{-8}$	400	7.4
Al_2O_3	7.54 $x10^{-8}$	95	8
TiO_2	18.5 $x10^{-8}$	180	38

Table 1. Tabulation of the capacitance of the insulator (C_i), dielectric thickness, and the dielectric constant (ε) of each insulator studied.

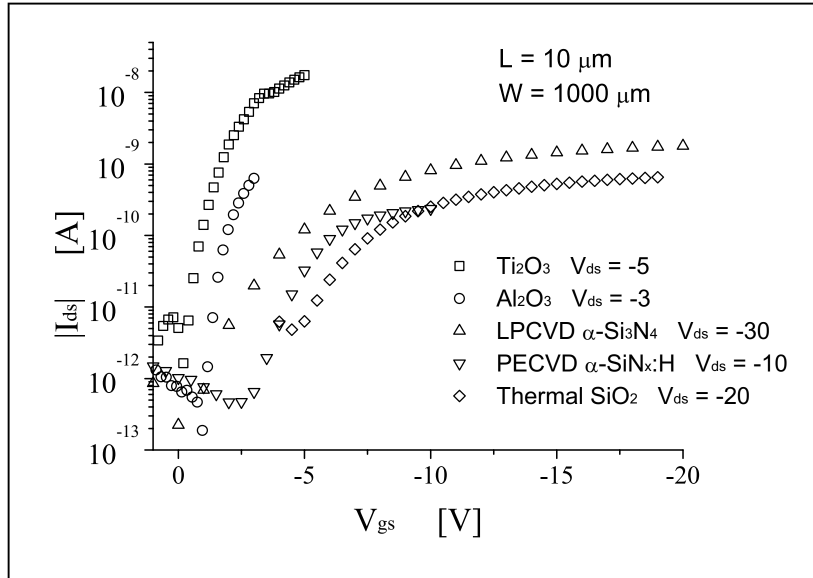

Figure 3. Transfer characteristics (I_{ds} verses V_{gs}) in the saturation regime for the P-TFTs with different gate dielectrics are shown.

A plot of the transfer characteristics for all the dielectrics is shown Figure 3. Note that for TiO_2 and Al_2O_3 P-TFT's operate at lower gate and drain voltages than for the silicon nitrides and thermal silicon oxide. This was the expected result of the greater C_i for TiO_2 and Al_2O_3. The TiO_2 and Al_2O_3 P-TFTs could not be forced to higher voltages, however, as leakage current would then be too large in these devices. Hence, the Al_2O_3 device did not quite reach true device saturation operation. Based on the shape of the transfer characteristics, the TiO_2 device just reached saturation. The linear portion of the transfer characteristics curve can be fitted to Equation 1. Using this equation the subthreshold slope [16] (S) can be obtained.

$$S = \left(\frac{dLog(I_{ds})}{dV_{gs}} \right)^{-1} \quad (1)$$

	ε	V_{th} (V)	Qth (C/cm^2)	Mobility (cm^2/Vs)	S (V/dec)	N_{ss}^{max} (cm^{-2} eV^{-1})
TiO_2	38	-0.36	-6.6 x10^{-8}	4.7 x10^{-5}	0.3	5.5 x10^{12}
Al_2O3	8	-1.2	-8.9 x10^{-8}	5.1 x10^{-5}	0.3	2.2 x10^{12}
LPCVD α–Si_3N_4:H	7.4	-2.0	-3.4 x10^{-8}	1.7 x10^{-5}	1.5	2.5 x10^{12}
PECVD α–SiN_x:H	7.2	-3.4	-5.4 x10^{-8}	1.6 x10^{-5}	1.3	1.9 x10^{12}
SiO_2	3.7	-4.2	-6.8 x10^{-8}	1.0 x10^{-5}	2.0	3.3 x10^{12}

Table 2. Tabulation of dielectric constant (ε), threshold voltage (V_{th}), threshold charge (Q_{th}), mobility, subthreshold slope (S), and maximum number of interface traps (N_{ss}^{max}).

It is evident that the linear portion of the transfer curves for TiO_2 and Al_2O_3 has much steeper slopes. This slope can be thought of as the rate at which traps are filled. All the traps must be filled before free charges can begin to cross the channel from the source to the drain. The steeper the slope of the curve, the lower the values for S will be, meaning the devices will reach an ON current at much lower voltages than for devices with higher S values.

The low S values of TiO_2 and Al_2O_3 are attributable to their high C_i. The values of S are found in Table 2.

To compare the performance of devices using gate dielectrics with different dielectric constants, normalization of the transfer characteristics to charge [16] is needed. The electrical charge (Q_i) induced by the gate insulator at he F8T2-gate insulator interface (in C/cm^2) is given by $Q_i = C_i * V_{gs}$. Figure 4 shows the I_{ds} verses Q_i curve. The curves do not perfectly collapse upon one another, but it can be seen that, upon normalizing for charge, the devices all operate consistently. From this figure we can conclude that F8T2 P-TFT performance is controlled by the quality of the F8T2 rather than the quality of the F8T2-gate dielectric interface, although a slightly larger I_{ds} is observed for TiO_2 at higher Q values.

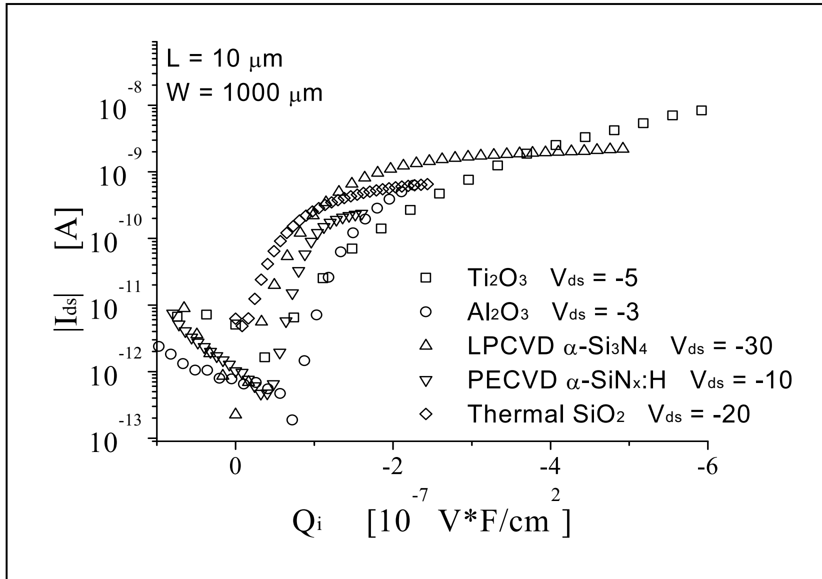

Figure 4. Transfer characteristics in the saturation regime normalized to charge (I_{ds} verses Q_i) to compare device operation across the studied dielectrics at equivalent charge.

A significant increase or decrease in interface traps could cause device performance to vary across dielectrics. From the subthreshold slope calculation, additional anaylsis can be done. The maximum number of interface traps (N_{ss}^{max}) [17] present can be calculated as shown in Equation 2.

$$N_{ss}^{max} = \left(\frac{S * Log(e)}{kT/q} - 1 \right) \frac{C_{ins}}{q} \quad (2)$$

Values for N_{ss}^{max} are found in Table 2. From the table we conclude that the best F8T2-gate dielectric interface, i.e. lowest N_{ss}^{max} value, in our devices is realized with the PECVD α-SiN_x:H. The highest value of N_{ss}^{max} is obtained for the TiO_2 gate dielectric.

Since the dielectrics have different surface energies and properties, we expect the polymer to interact with each dielectric in a different way. The values obtained for N_{ss}^{max} are different for the different gate dielectrics, but the difference is not very large, indicating that the differences in the F8T2-gate dielectric interfaces are not very large. This would also indicate that the P-TFT operation is controlled by bulk traps in the active region more than by interface traps. Since, in the top source/drain contact configuration the charge must pass through the bulk of the F8T2 to reach the active channel region at the polymer dielectric interface, it is possible that the bulk properties of the F8T2 could dominate our P-TFT characteristics. Details on this subject will be reported elsewhere.

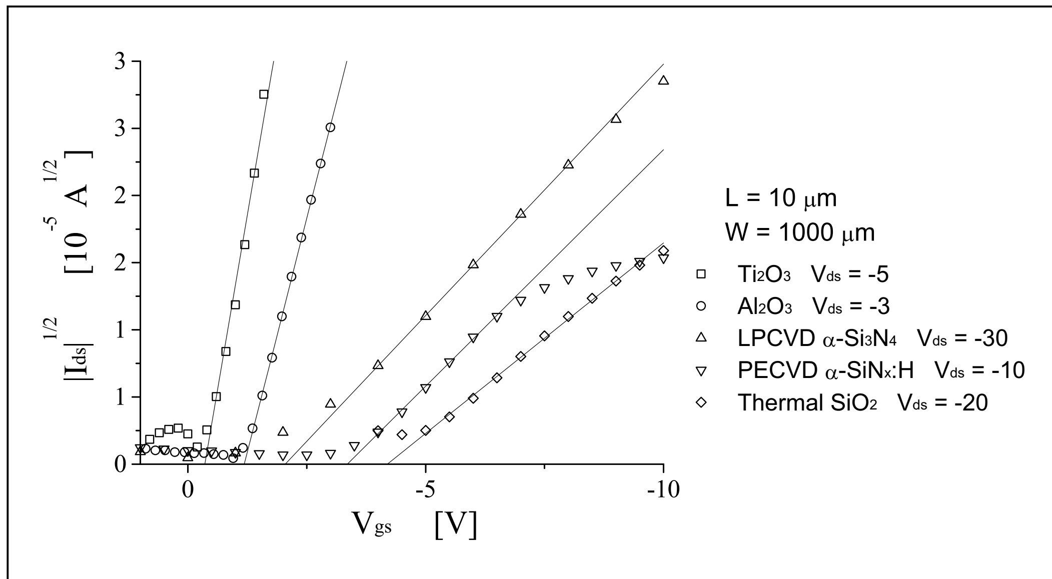

Figure 5. Analysis of the saturation regime transfer characteristics ($I_{ds}^{1/2}$ verses V_{gs}). μ_{FE} and V_{th} can be obtained from analysis of the linear portion of the curve.

Analysis of the transfer characteristics is shown in Figure 5 plotting $|Ids|^{1/2}$ verses V_{gs}. By fitting Equation 3, which was developed for the gradual channel aproximation[18], to the linear region of the curve, threshold (V_{th}) voltage and field-effect mobility (μ_{FE}) can be calculated.

$$\sqrt{I_{ds}} = \sqrt{\mu_{FE} C_{ins} \frac{W}{2L}} (V_{gs} - V_{th}) , \qquad (3)$$

Table 2 lists these parameters as well. The V_{th} in P-TFTs compares to the threshold for carrier conduction within the channel. TiO_2 has the lowest value of V_{th}. This is consistent with the low voltage operation expected for the large C_i that results from the TiO_2 gate dielectric. V_{th} can be normalized to charge (Q_{th}) and thought of as the threshold for charge for injection. Upon normalization, Table 2 shows that Q_{th} is about the same for all gate dielctrics, having an average value of -6.2 x10^{-8} C/cm^2. If we assume that Q_{th} is related to the filling of traps within F8T2, this would be comparable to an average trap density of about 3.9 x10^{11} cm^{-2} for F8T2. In future work, the location and energy of these traps will be investigated.

The similar Q_{th} for F8T2 on different dielectrics is consistent with the fact that the same material, F8T2, was used for all devices. If bulk trap states in the F8T2 make up the largest percentage of traps present, then the bulk properties of F8T2 will dominate the device characteristics across dielectrics. The small differences in Q_{th} could also be explained by the difference in interface traps between F8T2 and the different dielectrics. A greater number of interface traps would lead to a greater value for Q_{th} because these traps would have to be filled before the device could be turned on.

The calculated μ_{FE} values are listed in Table 2. These μ_{FE} values were obtained on the native dielectric surface. Others have shown that forming monolayers on the dielectric surface enhances mobility[19, 20], presumably due to a better polymer-dielectric interface, possibly a reduction in interface traps. We purposefully did not perform any monolayer formation treatments. We wanted to analyze the native dielectric properties. In fact, our top contact fabrication procedure was conducive to this goal, in that photolithographic electrode patterning never compromised the dielectric. The F8T2 was spun directly onto a cleaned, native dielectric. These μ_{FE} values are consistent with those reported recently by groups using F8T2 in which monolayer treatments on the gate dielectric surface were not performed [16, 20].

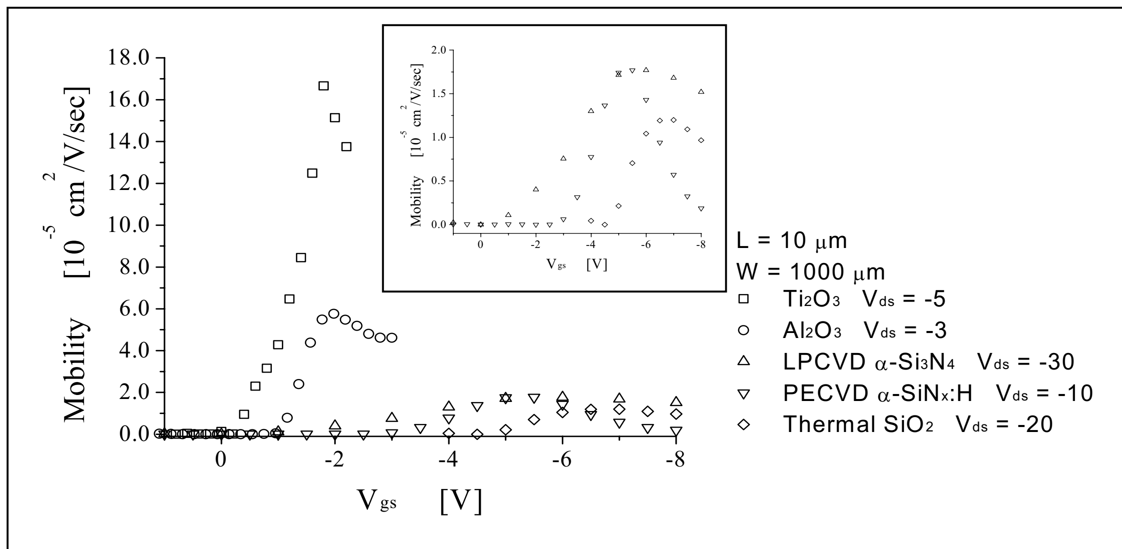

Figure 6. Variation of μ_{FE} verses V_{gs} shows that μ_{FE} reaches a maximum before carries are scattered as they cross the channel

A comparison of μ_{FE} verses V_{gs} can be seen in Figure 6. This graph was generated using Equation 4 [21].

$$\mu = \left(\frac{d\sqrt{I_{ds}}}{d(V_{gs} - V_{th})} \right)^2 * 2L/CiW, \quad (4)$$

The graph shows that the when the device reaches the ON state, μ_{FE} saturates and then begins to decrease. The decrease in μ_{FE} can be attributed to the scattering of carries by charges trapped at the polymer-dielectric interface or in the bulk. The saturation mobility values are consistent with the calculated values reported in Table 2.

4. CONCLUSION

For the first time, stable P-TFTs have been produced by photolithographic patterning of top source/drain contacts on F8T2 semiconducting polymer. The top contacts geometry reduced leakage current to a functional level for leaky high dielectric constant (ε) materials. Low voltage operation for P-TFTs was shown with higher dielectric constant (ε) gate insulators due to the large charge present across the dielectric. At equivalent gate charge, mobility values from the various dielectrics are consistent with one another, indicating that the bulk properties of the F8T2 are the main contributors to device operation with less influence from interface states.

5. ACKNOWLEDGMENTS

We would like to thank and acknowledge Dow Chemical for providing the F8T2 used in this study.

We would like to thank and acknowledge Symmorphix (Santa Clara, CA) for providing the TiO_2 and Al_2O_3 used in this study.

Research at UCSB was supported by the Air Force Office of Scientific Research (F49620-02-1-0127); Dr. Charles Lee, Program Officer.

6. REFERENCES

1. B. C. Bartic, H. Jansen, A. Campitelli, and S. Borghs, "Ta_2O_5 as gate dielectric material for low-voltage organic thin-film transistors," *Organ. Electron.* **3**, 65-72 (2002).
2. L.A. Majewski, M. Grell, S.D. Ogier, and J. Veres, "A novel gate insulator for fexible electronics," *Organ. Electron.* **4**, 27-32 (2003).
3. C. D. Dimitrakopoulos, I. Kymissis, S. Purushothaman, D, Neumayer, P. Duncombe, and R. Laibowitz, "Low-Voltage, High-Mobility Pentacene Transistors with Solution-Processed High Dielectric Constant Insulators," *Adv. Mater.* **11**, 1372-1375 (1999).
4. J. A. Rogers, Z. Bao and V. R. Raju, "Nonphotolithographic fabrication of organic transistors with micron feature sizes" *Appl. Phys. Lett.* **72**, 2716-2718 (1998).
5. M. Matters, D. M. de Leeuw, M. J. C. M. Vissenberg, C. M. Hart, P. T. Herwig, T. Geuns, C. M. J. Mutsaers and C. J. Drury, "Organic field-effect transistors and all-polymer integrated circuits" *Opt. Mater.* **12**, 189-197 (1999).
6. J. H. Lee, S. H. Kim, G. H. Kim, J.-I. Lee, Y. S. Yang, H. Y. Chu, J. Oh, L.-M. Do and T. Zyung, "Organic Transistors Using Polymeric Gate Dielectrics," *J. Korean Phys. Soc*. **42**, S614-S617 (2003).
7. F. Garnier, R. Hajlaoui, A. Yassar, and P. Srivastava, "All-polymer field-effect transistor realized by printing techniques," *Science* **265**, 1684-1686 (1994).
8. Z. N. Bao, Y. Feng, A. Dodabalapur, V. R. Raju, and A. J. Lovinger, "High-performance plastic transistors fabricated by printing techniques," *Chem. Mater.* **9**, 1299-1301 (1997).
9. A. Kumar and G. M. Whitesides, "Features of gold having micrometer to centimetre dimensions can be formed through a combination of stamping with an elastomeric stamp and an alkanethiol 'ink' followed by chemical etching," *Appl. Phys. Lett.* **63**, 2002-2004 (1993).
10. J. A. Rogers, Z. N. Bao, A. Makhija, and P. Braun, "Printing process suitable for reel-to-reel production of high-performance organic transistors and circuits," *Adv. Mater.* **11**, 741-745 (1999).
11. T. R. Hebner, C. C. Wu, D. Marcy, M. H. Lu, and J. C. Sturm, "Ink-jet printing of doped polymers for organic light emitting devices," *Appl. Phys. Lett.* **72**, 519-521 (1998).
12. C. M. Hong, S. Wagner, "Inkjet printed copper source/drain metallization for amorphous silicon thin-film transistors," *IEEE Elec. Dev. Lett.* **21**, 384-386 (2000).
13. H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E. P. Woo, "High-Resolution Inkjet Printing of All-Polymer Transistor Circuits," *Science* **290**, 2123-2126 (2000).
14. R. A. Street and A. Salleo, "Contact effects in polymer transistors," *Appl. Phys. Lett.* **81**, 2887-2889 (2002).
15. J. Swensen, J. Kanicki, A. Heeger (in publication process 2003)
16. S. Martin, J. Nahm, and J. Kanicki, "Gate-planarized organic polymer thin film transistors," *J. Elect. Mater.* **31**, 512-519, (2002).
17. A. Rolland, J. Richard, J.-P. Kleider, and D. Mencaraglia, "Electrical properties of amorphous silicon transistors and MIS-devices: comparative study of top nitride and bottom nitride configurations," *J. Electrochem. Soc.* **140**, 3679-3684 (1993).
18. R. F. Pierret, *Modular Series on Solid State Devices*, vol. IV, Addison-Wesley Pub. Co., Reading, MA, (1990).
19. Y.-Y. Lin; D. I. Gundlach, S. F. Nelson, and T. N. Jackson, "Pentacene-based organic thin-film transistors," *IEEE Trans. Electrton. Dev.* **44**, 1325-1331 (1997).
20. Salleo A, Chabinyc ML, Yang MS, Street RA, "Polymer thin-film transistors with chemically modified dielectric interfaces," *Appl. Phys. Lett.* **81**, 4383-4385 (2002).
21. Z. Bao, A. J. Lovinger, and A. Dodabalapur, "Organic field-effect transistors with high mobility based on copper phthalocyanine," *Appl. Phys. Lett.* **69**, 3066-3068 (1996).