2.2: Electrical Instabilities and Relaxation of Organic Polymer Thin-Film Transistors

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Abstract

We have studied the electrically induced instabilities of gate-planarized organic polymer thin-film transistors using spin-coated F8T2 organic polymer. We show that the main consequence of the electrical instabilities is a shift of the threshold voltage. We performed conventional bias temperature stress experiments under different stress conditions and investigated the variations of the resulting threshold voltage shift. We also present an analysis of the relaxation phenomenon that occurs after the electrical stress is interrupted.

1. Introduction

OP-TFTs have a considerable potential in large-area low-cost flexible electronics and they are becoming more and more attractive to flat panel display addressing applications. However, the details of their operation are still a matter of discussion and improvements of their electrical performance are still needed. In addition, it has been observed by many authors that the device performance can change significantly with time because of the electrical instabilities of the devices. The electrical stability of OP-TFTs is an important factor regardless of which application is considered. In active matrix flat panel display addressing, a threshold voltage shift of the OP-TFT could reduce the pixel luminance unless it is compensated by specific pixel electrode circuits.

2. Device fabrication and electrical performances

The device structure used in this study is an inverted staggered, gate-planarized TFT with bottom source / drain contacts fabricated on c-Si substrates covered with 1μm-thick SiO_2. A schematic cross section of the device is shown in Figure 1.
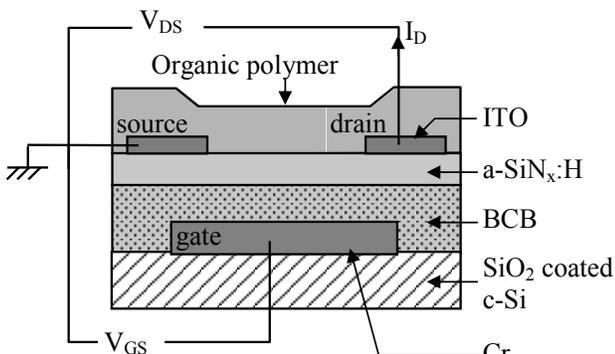
Figure 1: Schematic cross-section of our gate-planarized OP-TFTs.

The organic semiconductor used here is based on a solution of poly(9,9-dioctylfluorene-co-bithiophene) (F8T2) [1,2,3]. The F8T2 polymer used in this study has a weight-average molecular weight (Mw) of about 50 000.
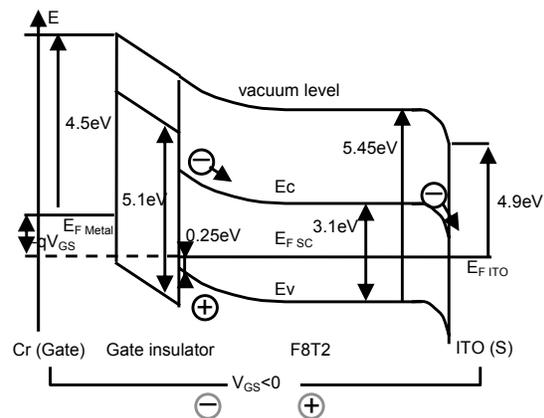
Figure 2: Proposed band diagram of the OP-TFT structure perpendicular to the source-drain axis, when the device is in the accumulation regime.
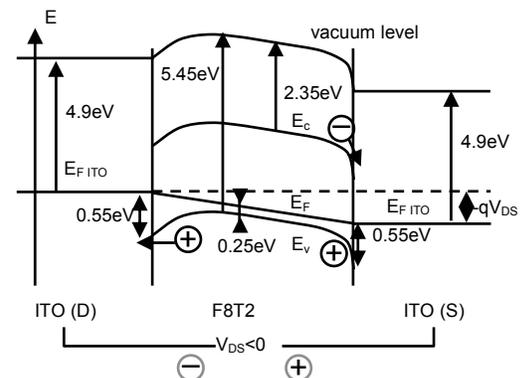
Figure 3: Proposed band diagram of the OP-TFT structure along the source-drain axis, when the device is in the accumulation regime and when $V_{DS}<0$.

Figure 2 and Figure 3 show the band diagram of our OP-TFT structure perpendicular to the interfaces and along the source-drain axis, respectively. Under accumulation, the band diagram perpendicular to the source-drain axis is similar to what we expect for TFTs based on inorganic semiconductors. Along the source-drain axis, we believe that we have Schottky source and drain contacts in our OP-TFTs [4]. In the accumulation regime and under a negative source-drain voltage, we can have extraction of

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electrons from the semiconductor to the ITO source electrode. Although the exact theory of OP-TFT operation is still under investigation, the MOSFET theory as modified for amorphous semiconductor-based TFTs provides a good initial description of the device behavior. Consequently, we extract the TFT field-effect mobility and threshold voltage in the linear regime at low source-drain voltage from the following equation:

$$I_{DS} = -\mu_{FE\ lin} C_{ins} \frac{W}{L} \left(V_{GS} - V_{T\ lin} \right) V_{DS} \tag{1}$$

In the saturation regime, we use:

$$I_{DS} = -\mu_{FE\ sat} C_{ins} \frac{W}{2L} \left(V_{GS} - V_{T\ sat} \right)^2 \tag{2}$$

The OP-TFT subthreshold swing S is extracted from [5]:

$$I_{DS} \propto 10^{-V_{GS}/S} \tag{3}$$

Typical electrical parameters of our devices are summarized in Table 1. We should note that, because the OP-TFTs do not always perfectly follow the MOSFET equations (1) and (2), it is often necessary to include the gate voltage dependence of the field-effect mobility in the equations describing the device operation. More precisely, we can use an additional parameter γ [6] to modify the equations for the linear and saturation regimes as follows:

$$I_{DS} = -\mu_{FE\ lin} C_{ins} \frac{W}{L} \left(V_{GS} - V_{T\ lin} \right)^{\gamma} V_{DS} \tag{4}$$

and $I_{DS} = -\mu_{FE\ sat} C_{ins} \frac{W}{(\gamma+1)L} \left(V_{GS} - V_{T\ sat} \right)^{\gamma+1}$ (5)

The parameter γ has been associated, in *n*-channel inorganic amorphous semiconductor devices, with the density of states in the semiconductor, and more precisely the characteristic temperature of the conduction band tail. However, further analysis is needed to explain values of γ larger than 1 in the case of organic semiconductor devices.

Table 1: Typical electrical parameters of our OP-TFTs

W/L	56/16
Ci (F/cm^2)	7.5×10^{-9}
$\mu_{FE\ lin}$ (cm^2/Vs)	1.5×10^{-3}
$V_{T\ lin}$ (V)	-16.5
$V_{T\ lin\ norm}$ (C/cm^2)	-1.2×10^{-7}
γ	1.5
$\mu_{FE\ sat}$ (cm^2/Vs)	3.5×10^{-3}
$V_{T\ sat}$ (V)	-16.5
$V_{T\ sat\ norm}$ (C/cm^2)	-1.2×10^{-7}
S (V/dec)	1.5
$N_{ss}^{max} = \left(\frac{S \log(e)}{kT/q} - 1 \right) \frac{C_i}{q}$ (cm^{-2}eV^{-1})	1.2×10^{12}
ON/OFF ratio (in linear regime)	10^5

3.   Bias-temperature stress experiments

Conventional bias temperature stress (BTS) experiments have also been performed, in which the device is subjected to a constant (DC) gate bias during a given stress time, at a given stress temperature. At several pre-selected times, the stress is interrupted and the transfer characteristics in the linear regime is measured before resuming the electrical stress. Transfer characteristics obtained after such a stress at room temperature are shown in Figure 4 and Figure 5. We can clearly see in the figures below that a negative BTS, during which the device is in the accumulation regime, has a very large effect on the threshold voltage but does not significantly affect the field-effect mobility or subthreshold swing. This is consistent with BTS experiments performed on inorganic devices. On the other hand, after a positive BTS, during which the device is in the OFF-state, the electrical characteristics are severely degraded, especially the subthreshold swing.
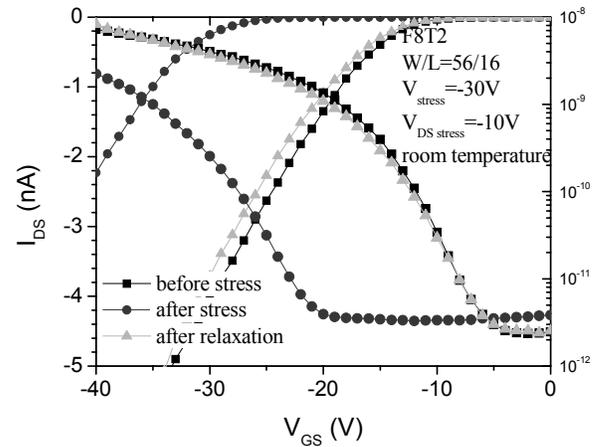
Figure 4: OP-TFT transfer characteristics before and after negative bias stress experiment. Also shown is the transfer characteristic after device relaxation.
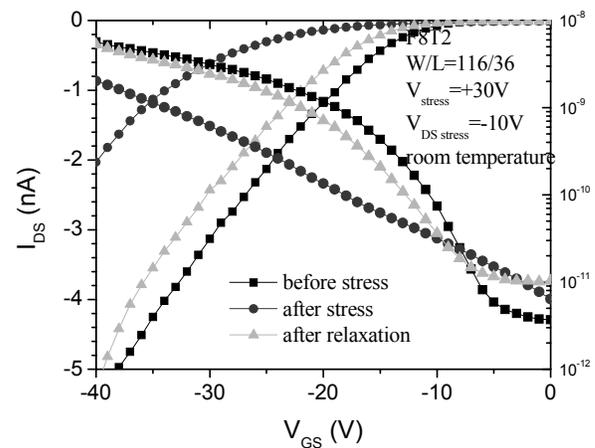
Figure 5: OP-TFT transfer characteristics before and after positive bias stress experiment. Also shown is the transfer characteristic after device relaxation

We should note that, in both cases, the device electrical performances are restored after relaxation. Further details on this

subject are presented later in this paper. In this study, we have focused on the negative electrical stress experiments. More precisely, we have investigated the dependence of the threshold voltage shift obtained after negative bias temperature stress with the stress parameters, i.e. stress time, stress voltage and stress temperature. The threshold voltage shift is defined as:

$$\Delta V_T(t) = V_T(t) - V_T(t=0) \tag{6}$$

where $V_T(t)$ is the threshold voltage extracted from the transfer characteristics of the OP-TFT in the linear regime, according to equation (1), at the stress time t. It should be noted that this value is roughly similar to the voltage shift obtained by looking at a constant current in the subthreshold regime of the transfer characteristics. We have observed that the threshold voltage shift versus stress time curves can be fitted by the following stretched exponential equation, based on the analysis developed for a-Si:H TFTs [7]:

$$\Delta V_T = B\left(1 - \exp\left[-\left(\frac{t}{\tau}\right)^\beta\right]\right) \tag{7}$$

where B, β and τ are fitting parameters that can depend on the stress voltage and stress temperature. In a-Si:H TFTs, B depends mostly on the stress voltage and has often been expressed as one of the following equations:

$$B = (V_{ST} - V_{Ti}) \text{ or } B \propto (V_{ST} - V_{Ti})^\alpha \tag{8}$$

where α is a parameter associated with the semiconductor density of states [7,8]. For low temperature values, the fitting parameter β increases linearly with the stress temperature [7]:

$$\beta = T_{stress}/T_0^* - \beta_0 \tag{9}$$

where β_0 and T_0^* are material-dependent parameters. For stress temperature values higher than about 80°C, β saturates. The fitting parameter τ exhibits a power law dependence with the stress voltage [8]. In addition, τ has been shown [7] to be activated in temperature with an activation energy $-E_\tau$ associated with the barrier energy that the carriers need to overcome before they can be injected into the gate insulator.

Figure 6 and Figure 7 show our experimental data obtained for OP-TFTs subjected to different BTS conditions and the corresponding fits to equation (7). We can see that we have obtained very acceptable fits using this equation for a wide range of stress voltages and stress temperatures.
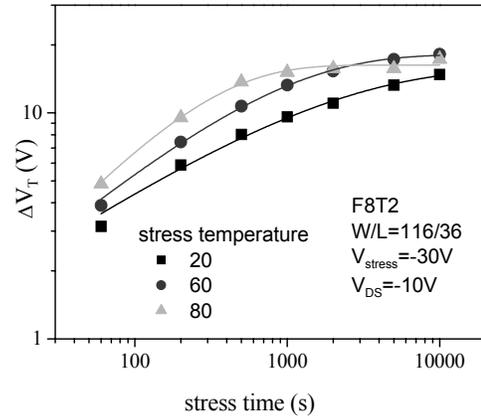
Figure 7: Threshold voltage shift at different stress temperature and constant stress voltage. Symbols show experimental data, lines show fit to the stretched exponential equation.

We have also investigated the effect of the stress voltage and stress temperature on the three fitting parameters. We have observed that B increases with the stress voltage, as shown in Figure 8 and is stress temperature-independent. The parameter β is roughly independent of the stress voltage and increases with the stress temperature, as shown in Figure 9. The parameter τ decreases with both stress voltage and stress temperature. However, further BTS experiments are needed to describe more accurately the exact variations of these parameters.
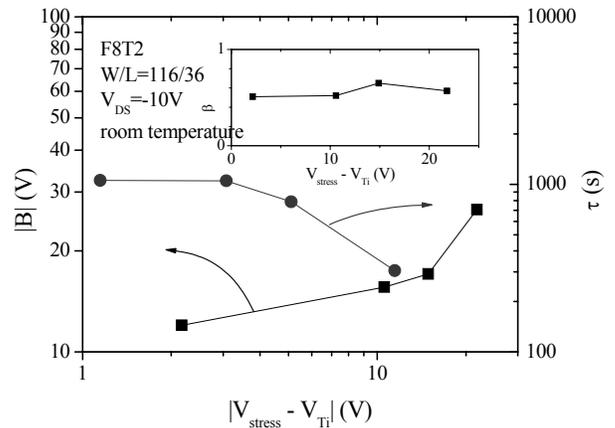
Figure 8: Variations of the three fitting parameters used in Figure 6 with the stress voltage above the initial threshold voltage.

Figure 6: Threshold voltage shift at different stress voltages and constant stress temperature. Symbols show experimental data, lines show fit to the stretched exponential equation.
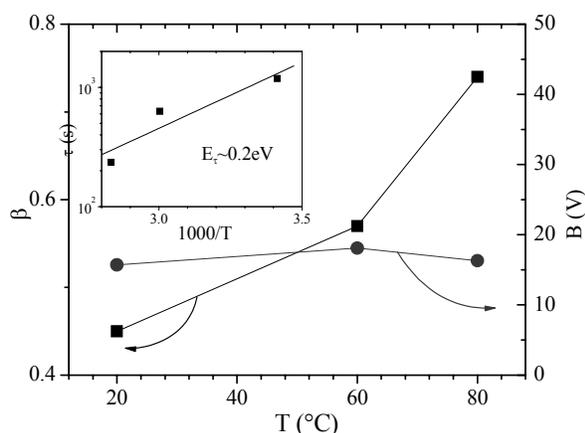
Figure 9: Variations of the three fitting parameters used in Figure 7 with the stress temperature.

4. Device relaxation after electrical stress

We should note that, after the bias stress is removed, the device relaxes towards its initial state, as shown in Figure 10. In this figure, we have plotted the threshold voltage shift measured after the BTS was interrupted, for different devices and different stress conditions. The time $t=0$ corresponds to the end of the BTS and a threshold voltage shift $\Delta V_T=0$ corresponds to the initial state of the device, before the start of the BTS experiment.
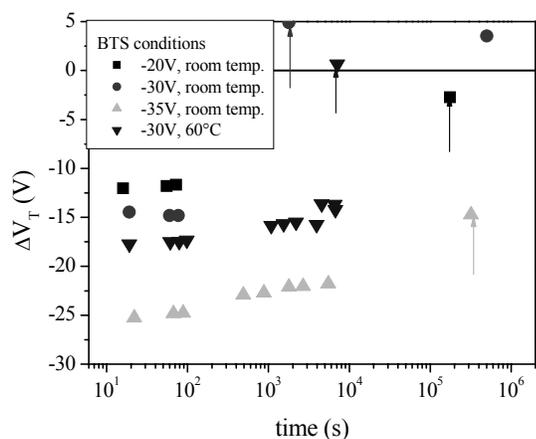
Figure 10: Reversal of threshold voltage shift during device relaxation after BTS experiment.

We can see in Figure 10 that the device relaxes back to initial state, even at room temperature. We have investigated the effect of illumination on this relaxation. To do so, we illuminated our devices for a few seconds with a broadband light source (halogen bulb 150W). The typical power density reaching the device is about 260 mW/cm^2, but it should be noted that most of this power corresponds to a portion of the light spectrum that is not absorbed by the semiconductor. In each case, we measured the device immediately after having subjected it to illumination. The corresponding threshold voltage shift is shown on the curves in Figure 10 with an arrow. We can see that the device relaxation is very significantly accelerated by illumination, which is consistent

with a recently published study [9]. However, further experiments are needed to accurately describe the relaxation of our devices, especially its speed and illumination wavelength dependence.

This relaxation back to the device initial state suggests that the mechanisms responsible for the OP-TFTs threshold voltage shift involve trapping of carriers in the organic semiconductor, probably near the gate insulator interface, most likely into shallow defect states. This mechanism seems more likely than creation of defects in the organic semiconductor or carrier injection into the gate insulator. By analogy with the analysis performed for a-Si:H TFTs [7], the activation energy of the parameter τ, shown in the inset of Figure 9, could be associated with the energy of the defect states involved in the carrier trapping. Further experiments are needed to confirm this theory.

5. Conclusion

We have characterized the electrical instabilities of our gate-planarized thin-film transistors based on F8T2. We presented the effect of both positive and negative stress voltages and showed that positive BTS significantly degrades the device characteristics while negative BTS mainly results in a threshold voltage shift. We described the threshold voltage shift dependence on stress time, voltage and temperature for negative BTS experiments, using a model based on the stretched exponential equation. In addition, we observed that our devices relax back to their initial state after the BTS is over, and that this relaxation is significantly accelerated by illumination. We concluded that the electrical instabilities of our OP-TFTs are most likely associated with trapping into shallow defect states in the organic semiconductor.

Acknowledgements

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