Organic-polymer thin-film transistors for active-matrix flat-panel displays?

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Abstract — Organic-polymer-based thin-film transistors (OP-TFTs) look very promising for flexible, large-area, and low-cost organic electronics. In this paper, we describe devices based on spin-coated organic polymer that reproducibly exhibit field-effect mobility values around 5×10^{-3} cm^2/V-sec. We also address fabrication, performance, and stability issues that are critical for the use of such devices in active-matrix flat-panel displays.

Keywords — *Thin-film transistors, organic polymers, series resistances, field-effect mobility, flat-panel displays, active-matrix LCDs, active-matrix OLEDs.*

1 Introduction

Organic semiconductors can be divided into two main groups: oligomers and polymers.[1,2] In general, oligomers deposited by evaporation in vacuum have a highly ordered molecular structure whereas, most of the time, organic polymers (OP), deposited by spin coating or ink-jet printing at low temperature over large areas[3] are amorphous. Hence, organic-polymer thin-film transistors (OP-TFTs) usually show lower electrical performances than oligomer-based devices,[1] but often exhibit better stability in air and have a lower OFF-current. Both types of organic materials have a considerable potential in large-area low-cost flexible organics electronics. They can be deposited on flexible, light-weight polymeric substrates instead of conventional glass substrates[4] and, when fabricated in combination with organic-polymer light-emitting diodes (OP-LED), these devices can be used to make very attractive all-organic-polymer flexible-display systems.[5]

Thus far, most research groups have used device test structures, in which no patterning of the organic and inorganic (especially the gate electrode and insulator) layers is involved. State-of-the-art field-effect mobility values reported for OP-TFTs with patterned gate electrodes are typically in the range of 10^{-3}-10^{-1} cm^2/V-sec,[6] depending on device structure and material.

2 Device fabrication and electrical performances

We have fabricated and characterized gate-planarized OP-TFTs based on the structure shown in Fig. 1.[7] The devices use benzocyclobutene (BCB) as the gate-planarization material, amorphous-silicon nitride deposited by plasma-enhanced chemical vapor deposition (PECVD) as the gate insulator, and ITO as source and drain electrodes. Our typical TFT channel width and length are 50–100 and 6–100 μm, respectively. The organic semiconductors used here are based on solutions of poly(9,9-dioctylfluorene-co-bithiophene) (F8T2).[8–10] In this study, F8T2-1 has a higher weight-averaged molecular weight (Mw) than F8T2-2 (Mw = 50,000 and 33,000, respectively). The corresponding inherent viscosity values for the two polymers are 1.08 and 0.42 dL/g, respectively (THF, 25.0°C, 0.5 g/dL). In general, F8T2 exhibits a liquid-crystalline phase[8] and is thermally stable in the air up to 350–400°C. We have also fabricated and characterized devices made from the organic polymers used in green and red PLEDs,[11,12] and from phenyl-substituted poly(p-phenylene vinylene), also known as super yellow[13] and typically used as a PLED emissive material.

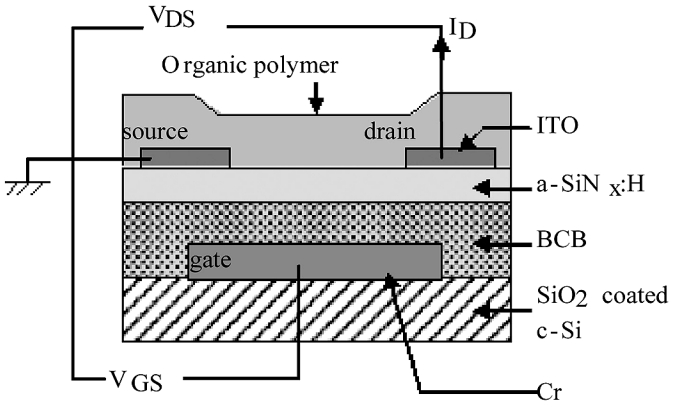

FIGURE 1 — Cross section of the gate-planarized OP-TFT structure used in this study.

Although the exact theory of OP-TFT operation is not yet fully known, the MOSFET theory as modified for amorphous-semiconductor-based TFTs provides a good initial description of the experimental data obtained for our OP-TFTs. Using this model, the OP-TFT field-effect mobility ($\mu_{FE\,lin}$) and threshold voltage ($V_{T\,lin}$) in the linear regime are extracted from the following equation:

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$$I_D = -\mu_{FE\,lin} C_i \frac{W}{L}\left[(V_{GS} - V_{T\,lin})V_{DS} - \frac{V_{DS}^2}{2}\right], \qquad (1)$$

or, for low V_{DS},

$$I_D = -\mu_{FE\,lin} C_i \frac{W}{L}\left(V_{GS} - V_{T\,lin}\right)V_{DS}, \qquad (2)$$

where C_i is the gate insulator capacitance per unit area, W is the channel width, and L is the channel length. In the saturation regime, the OP-TFT field-effect mobility ($\mu_{FE\,sat}$) and threshold voltage ($V_{T\,sat}$) are extracted from

$$I_D = -\mu_{FE\,sat} C_i \frac{W}{2L}\left(V_{GS} - V_{T\,sat}\right)^2. \qquad (3)$$

We should note that, to compare devices fabricated with different gate insulators (nature of material, thickness), we should use the equivalent charge or normalized threshold voltage $V_{T\,norm} = V_T \times C_i$ in both the linear and saturation regimes. In the weak accumulation regime, we can extract the device subthreshold swing (S) as defined below:

$$I_D \propto 10^{-V_{GS}/S}. \qquad (4)$$

From the subthresold swing S, we can also calculate the maximum density of states that can be present at the organic semiconductor/gate insulator interface,[14] $N_{ss}{}^{max}$:

$$N_{ss}^{\max} = \left(\frac{S\log(e)}{kT/q} - 1\right)\frac{C_i}{q}. \qquad (5)$$

Our devices were measured at room temperature, in air, using a Karl Suss PM8 probe station and an HP 4156A semiconductor parameter analyzer. The output characteristics were measured with the OP-TFT source grounded, the gate voltage held constant, and the drain voltage swept from 0 to negative. For the transfer characteristics, the source is grounded, the drain voltage is held constant, and the gate voltage is swept from negative to positive.[7] Typical OP-TFT transfer (drain current versus source-drain voltage) and output (drain current versus source-gate voltage) characteristics are plotted in Figs. 2(a) and 2(b), respectively. Figure 3 shows OP-TFT transfer characteristics in the linear and saturation regimes and the linear fits that were used to extract the device electrical parameters using Eqs. (1) and (3). We should note that, as we have observed in most cases, the field-effect mobility extracted in the saturation regime is slightly higher than the field-effect mobility extracted in the linear regime. In addition, we can see in Fig. 3 that the OP-TFT transfer characteristics do not exhibit the linear behavior predicted by the MOSFET equation for the linear regime. This deviation from the ideal MOSFET behavior is commonly observed in a-Si:H[15] and organic TFTs.[7,16] It has often been associated with the dispersive transport of carriers in the amorphous semiconductor.[15,17]

More precisely, the fundamental TFT equations for the linear regime can be modified to include an additional

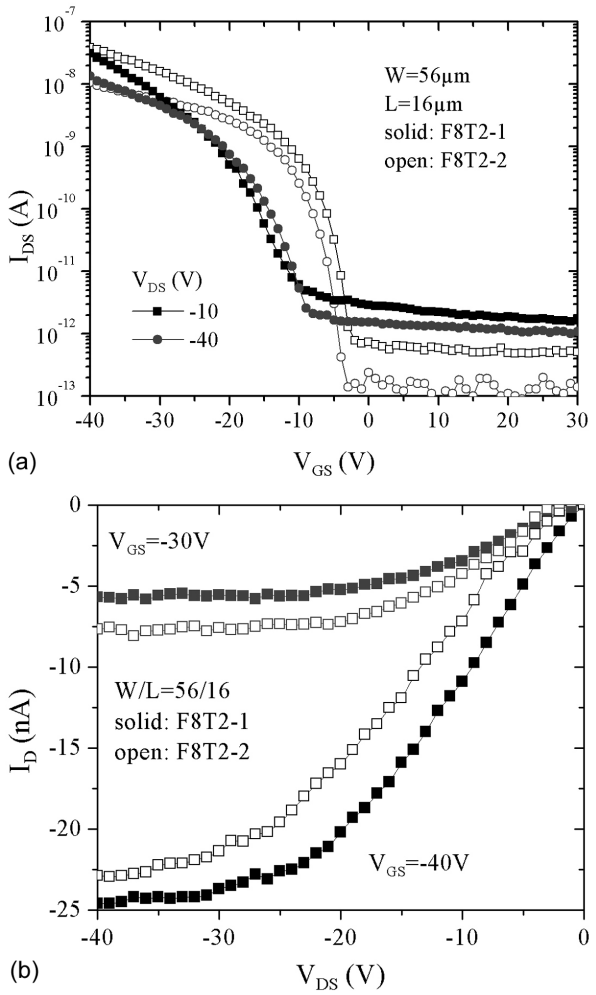

FIGURE 2 — (a) Typical transfer characteristics for F8T2-based OP-TFTs. (b) Output characteristics of the same devices.

parameter, γ, representative of the transfer characteristic non-linearity at low V_{DS}, as follows:

$$I_D = \mu_{0\,lin} C_i \frac{W}{L}\left(V_{GS} - V_T\right)^{\gamma} V_{DS}. \qquad (6)$$

In the saturation regime, the TFT equation becomes

$$I_D = \mu_{0\,sat} C_i \frac{W}{(\gamma+1)L}\left(V_{GS} - V_T\right)^{\gamma+1}, \qquad (7)$$

where $\mu_{0\,lin}$ and $\mu_{0\,sat}$ are fitting parameters associated with the field-effect mobility. In a-Si:H devices, γ is often defined as

$$\gamma = 2\frac{T_0}{T} - 1, \qquad (8)$$

where T is the temperature and T_0 is the characteristic temperature of the density-of-states distribution in the semiconductor around the position of the Fermi level.[18] Equation (8) is valid for $T < T_0$. In organic-polymer-based devices, the physical significance of values of the γ fitting parameter larger than 1 has not yet been fully explained. However, we believe that, following amorphous semicon-

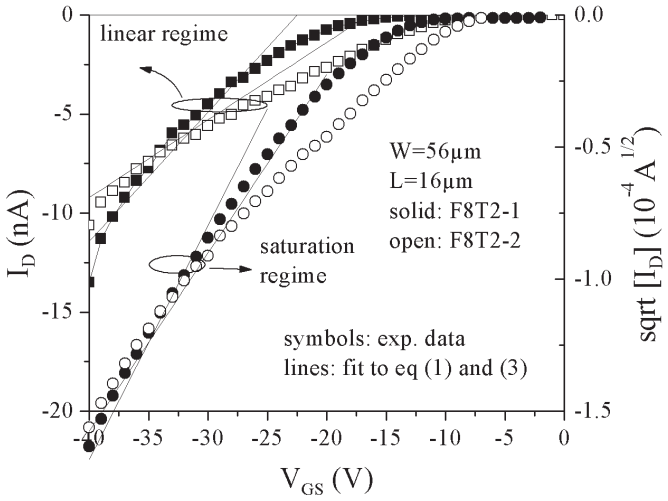

FIGURE 3 — Typical transfer characteristics for F8T2-based OP-TFTs in linear and saturation regimes. Symbols show experimental data and lines represent fit to Eqs. (1) and (3).

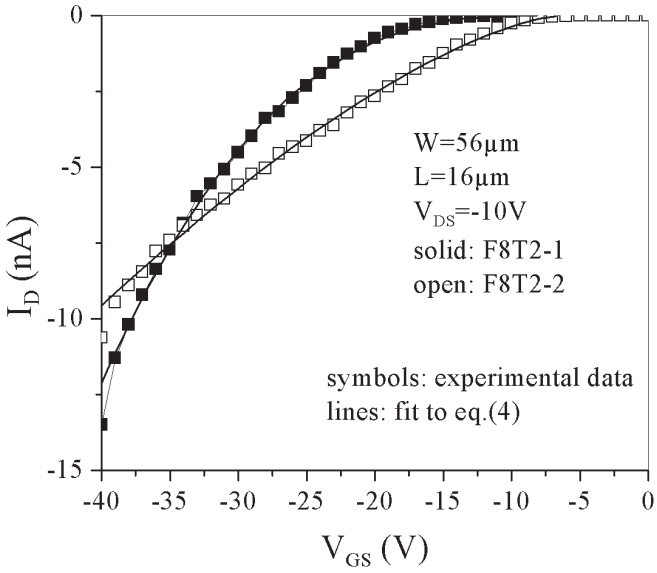

FIGURE 4 — Typical transfer characteristics for F8T2-based OP-TFTs in the linear regime and fit to Eq. (6).

ductor theory, it can also be associated with a high density of states around the Fermi level position, *i.e.*, most likely the density of valence band-tail states. It is also possible to observe apparent values of the γ fitting parameter lower than 1, because the parasitic source and drain series resistances can result in significant underestimation of γ.[19] We should note that the parameter γ used here corresponds to what some other research groups call γ + 1[20]: both models lead to the same equation in the linear regime for small source-drain voltages ($V_{DS} < V_{GS} - V_T$).

Figure 4 shows the OP-TFT transfer characteristics in the linear regime at low drain voltages along with the fits to Eq. (6). The γ values used for the fits are 2.7 and 1.5 for F8T2-1 and F8T2-2, respectively. We can clearly see that the fit is better using Eq. (6) than the standard MOSFET equation predicting a linear behavior. It should be noted that, if $\gamma \neq 1$, the unit of $\mu_{0\tau lin}$ and $\mu_{0\ sat}$ in Eqs. (6) and (7) is not $cm^2/V\cdot\cdot sec$. In this paper, for simplicity purposes, we will use the conventional equation (*i.e.*, $\gamma = 1$) for extraction of field-effect mobility and threshold-voltage values.

The electrical parameters obtained for each device are summarized in Table 1. In this table, we have also included the electrical performances of a typical gate-planarized a-Si:H TFT[21] for reference. We can clearly see that the best OP-TFT electrical performances have been obtained on devices based on F8T2, but that these performances are still significantly lower than those of a-Si:H TFTs, especially the field-effect mobility. Also, the best PLED material (super yellow) displayed the worst OP-TFT electrical performances.

We have investigated the OP-TFTs source/drain contacts behavior: although the electrical performances of

TABLE 1 — Typical electrical performances of OP-TFTs based on different organic polymers. Data on gate-planarized a-Si:H TFT is also included.

	F8T2-1	F8T2-2	OLED green[11]	OLED red[12]	Super yellow[13]	a-Si:H[21]
W/L	56/16	56/16	116/36	116/36	116/56	116/56
Ci (F/cm^2)	7.5×10^{-9}	7.5×10^{-9}	7.5×10^{-9}	7.5×10^{-9}	7.5×10^{-9}	2.4×10^{-9}
$\mu_{FE\ lin}$ (cm^2/V-sec)	2.5×10^{-3}	1.5×10^{-3}	3.7×10^{-5}	6×10^{-6}	1.7×10^{-5}	1.05
$V_{T\ lin}$ (V)	–21.5	–16.5	–11	–30	–61	29
$V_{T\ lin\ norm}$ (C/cm^2)	-2×10^{-7}	-1.2×10^{-7}	-8.25×10^{-8}	-2.25×10^{-7}	-4.5×10^{-7}	7×10^{-8}
γ	2.7 ± 0.2	1.5 ± 0.1	1.5	1.7	2.9 ± 0.1	1.24 ± 0.03
$\mu_{FE\ sat}$ (cm^2/V-sec)	6.0×10^{-3}	3.5×10^{-3}	5.1×10^{-5}	1.8×10^{-5}	1.92×10^{-5}	1.5
$V_{T\ sat}$ (V)	–21	–16.5	–8	–26	–55	15
$V_{T\ sat\ norm}$ (C/cm^2)	-1.6×10^{-7}	-1.2×10^{-7}	-6×10^{-8}	-1.95×10^{-7}	-4.1×10^{-7}	3.6×10^{-8}
S (V/dec)	2.8	1.5	5.5	2	5	0.9
$N_{ss}^{max}\left(\frac{S\log(e)}{kT/q}-1\right)\frac{C_i}{q}$ (cm^{-2}-eV^{-1})	2.2×10^{12}	1.2×10^{12}	4.3×10^{12}	1.5×10^{12}	4×10^{12}	2.2×10^{11}
ON/OFF ratio (in linear regime)	4×10^3	10^5	2×10^2	4×10^2	3×10^2	10^6

many organic thin-film transistors are often limited by the low conductivity of the organic semiconductor, the source and drain contacts play a predominant role in the device operation and it has clearly been found that they may have a critical effect on the device performance. In conventional inorganic TFTs or MOSFETs, the S/D electrodes form ohmic contacts to a highly doped semiconductor layer. In general, the most simple TFT device model therefore assumes that source and drain contacts are ohmic and do not limit carrier injection. However, non-ohmic S/D contacts were observed in some O-TFTs and carrier injection has recently been investigated[22–24]: it is now believed that S/D contacts in OP-TFTs form Schottky barriers to the channel region. In Schottky barrier OP-TFTs, the carriers can tunnel through the Schottky barrier by field emission under negative gate and drain voltages.

A preliminary investigation of the quantitative role of the source/drain (S/D) contacts can nevertheless be conducted using a method developed for amorphous-semiconductor thin-film transistors with ohmic contacts: the Transmission Line Method (TLM).[25–27] This method models the S/D contacts and access regions by gate-voltage-dependent series resistances. For OP-TFTs with non-ohmic S/D contacts, the calculated series resistance also depends on the source-drain voltage. This analysis is done when the TFT is in the linear regime, for low values of the S/D voltage. The equation describing the OP-TFT operation in linear regime at low V_{DS} becomes

$$I_D = -\mu_{FE\,\mathrm{int}} C_i \frac{W}{L}\left(V_{GS} - V_{T\,\mathrm{int}}\right)\left(V_{DS} - R_{S/D} I_D\right), \quad (9)$$

where $\mu_{FE\,int}$ and $V_{T\,int}$ are the OP-TFT intrinsic field-effect mobility and threshold voltage, *i.e.,* representative of the conduction channel, or ideal TFT only (without the parasitic S/D resistances). $R_{S/D}$ is the total series resistance (source and drain) of the TFT. In most devices, we expect significant parasitic S/D series resistances resulting from the S/D contact resistances. We should note that, in staggered OP-TFT structures (for instance top contact devices), we could also expect additional resistance contributions from the access regions between the S/D contacts and the conduction channel (access resistance).[25] In the OP-TFTs studied here, we expect the conduction channel to be created in the same plane as the source and drain electrodes, which should drastically reduce the access resistances. However, significant contact resistances can nevertheless degrade the OP-TFT performances, especially in the linear regime, *i.e.,* at low V_{DS}.

To characterize the S/D series resistance using the TLM, we measured a series of OP-TFTs with identical S/D contact characteristics and different channel lengths. The ON resistances (R_{ON}) of the devices are plotted as a function of the channel length, as shown in Fig. 5(a). Based on Eq. (9), we can write

$$WR_{ON} = \frac{V_{DS}}{I_D} = WR_{S/D} + WR_{channel} \quad (10)$$

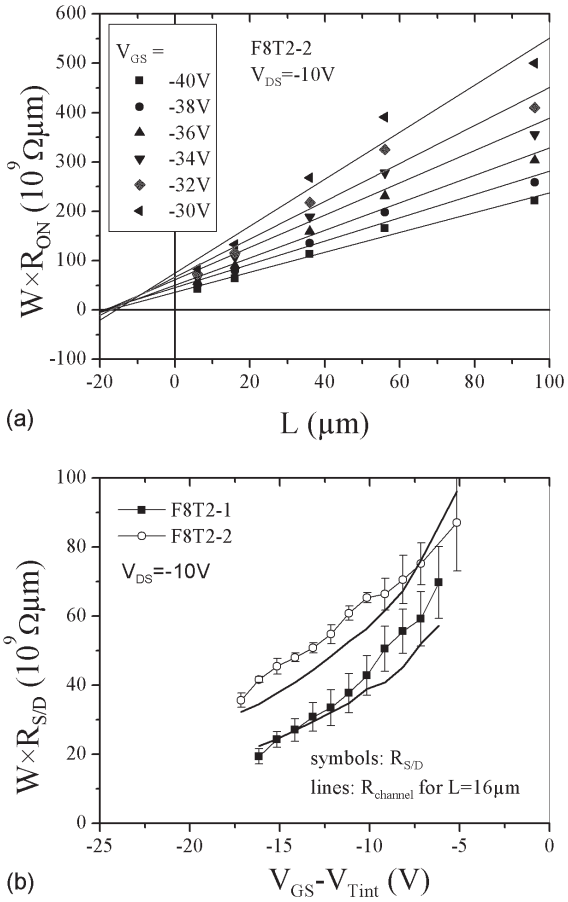

FIGURE 5 — (a) Total ON-resistance measured on a series of OP-TFTs based on F8T2-2. (b) Variations of the OP-TFT S/D series resistances and conduction channel resistance, extracted from (a), with the applied gate voltage.

with

$$R_{channel} = \frac{1}{\mu_{FE\,\mathrm{int}} C_i W\left(V_{GS} - V_{T\,\mathrm{int}}\right)} \times L. \quad (11)$$

The total S/D series resistance $R_{S/D}$ can therefore be extracted for each gate voltage from the y-intercept of the curves and the conduction channel resistance is calculated from the slope of the curves. Figure 5(b) shows the evolution of the total S/D series resistance and the corresponding values of the conduction channel resistance, for a channel length of L = 16 μm, extracted from the curves in Fig. 5(a). We obtained values of the S/D series resistance of around 4×10^8 and 6×10^8 Ω for F8T2-1 and Eq. (2), respectively, for V_{GT} around –10 V. We can see that for both polymers, the channel and S/D resistances are of comparable values, clearly indicating the significant effect of the S/D contacts on the overall electrical performance of the device. In addition, Eq. (12) shows that we can calculate the intrinsic field-effect mobility ($\mu_{FE\,int}$) and threshold voltage ($V_{T\,int}$) from the variations of the conduction channel resistance with V_{GS}, as illustrated in Fig. 6.

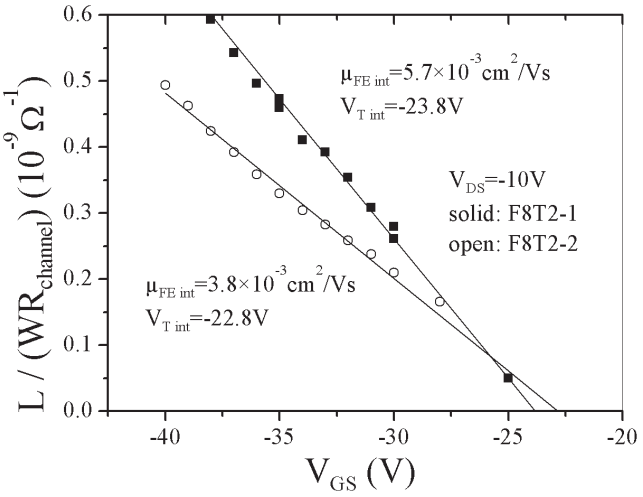

FIGURE 6 — Extraction of the OP-TFT intrinsic field-effect mobility and threshold voltage values.

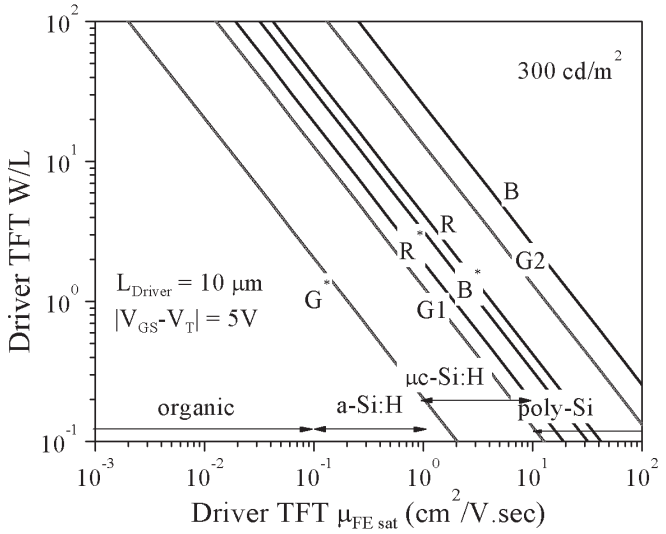

FIGURE 7 — Example of design requirements for the driver TFT in AMOLED for a display luminance of 300 cd/m^2 (Ref. 31).

$$\frac{L}{W \times R_{channel}} = \mu_{FE\,\mathrm{int}} C_i \left(V_{GS} - V_{T\,\mathrm{int}}\right). \qquad (12)$$

As expected, the intrinsic field-effect mobility is higher than the apparent field-effect mobility. This effect is more significant for short-channel devices since the channel resistance decreases with decreasing channel length while the S/D series resistances are channel length-independent.

3 All-organic active-matrix OP-TFT arrays

Although these results are extremely encouraging, we think that several issues, critical to the development of OP-TFT-based emissive or transmissive flat-panel displays (FPDs), need to be addressed before this technology can challenge existing inorganic TFT-driven flat-panel displays. In this paper, we will use active-matrix organic polymer light-emitting displays (AMPLED – emissive FPD) and active-matrix liquid-crystal displays (AMLCDs – transmissive FPD) as examples. Organic TFTs are already being investigated for the addressing of AMLCDs and small active-matrix reflective displays, based on PDLC technology, have been demonstrated using both polymer[28,29] and small molecule organic semiconductors.[30]

The level of ON-current that the OP-TFTs can provide is an important issue for active-matrix addressing in FPDs. PLEDs are sensitive to the current density, so the OP-TFT current requirement for AMPLED addressing increases with increasing PLED area. Today, the ON-current of OP-TFTs is too low for typical AMPLED driving conditions. As shown in Fig. 7, to reach acceptable ON-current values, the OP-TFT would typically have to be very large (*i.e.,* large W/L ratio),[31] which would reduce the pixel aperture ratio and therefore the display performance. High field-effect mobility and high dielectric-constant gate-insulator materials are therefore needed and top-light-emission PLEDs should be considered in combination with OP-TFTs. In AMLCDs, the OP-TFT current needs to be high enough so that the liquid crystal and storage capacitances can be fully charged during the available select time, which decreases with an increasing number of lines. Currently, the relatively low field-effect mobility obtained from polymer-based devices can limit the FPD resolution or its refresh rate. However, polymer-dispersed liquid-crystal-display (PDLC) and cholesteric liquid-crystal-display (Ch-LCD) active-matrix array requirements[32] can be compatible with the electrical performances of OP-TFTs.

The electrical stability of OP-TFTs is also a critical issue: we have shown that OP-TFTs often exhibit a significant threshold voltage shift, even after only moderate electrical stress.[33] Bias stress experiments have been performed, in which a constant (dc) gate bias is applied to the device during a given stress time at room temperature. At selected intermediate times, the stress is interrupted and a transfer characteristic is measured before resuming the electrical stress. Transfer characteristics obtained during such a stress, for a stress voltage of –30 V are shown in Fig. 8(a). We can clearly see that the stress experiment results in very significant threshold voltage shift while the field-effect mobility is not affected. We can also see that, after the stress experiment is stopped, the device electrical characteristic returns to its original state: this relaxation occurs within a few minutes at room temperature. Figure 8(b) shows the evolution of the field-effect mobility and threshold voltage shift as a function of the stress time. The threshold voltage shift is defined as

$$\Delta V_T(t) = V_T(t) - V_T(t=0), \qquad (13)$$

where $V_T(t)$ is the OP-TFT threshold voltage after a stress time t and $V_T(t = 0)$ is the threshold voltage before the bias stress experiment is started.

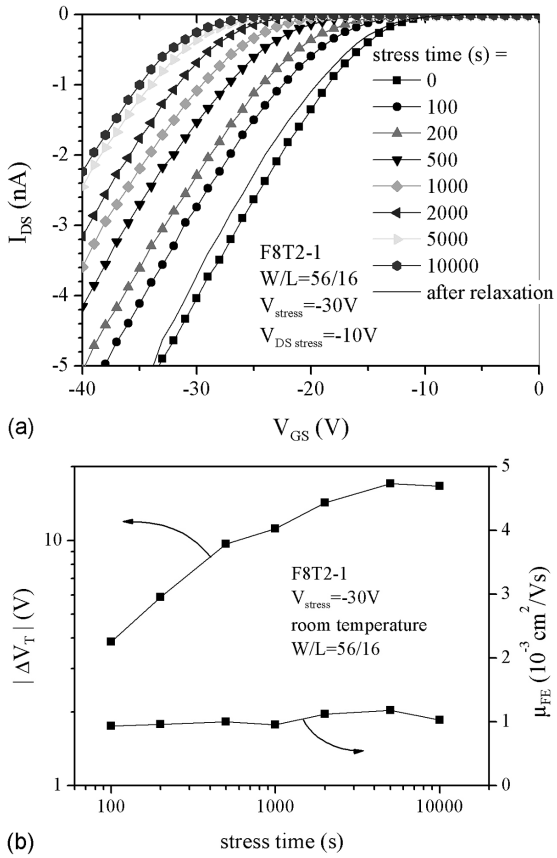

FIGURE 8 — (a) Transfer characteristics after bias stress experiments of different durations. (b) Threshold-voltage shift and field-effect mobility extracted form curves in (a) as a function of stress time.

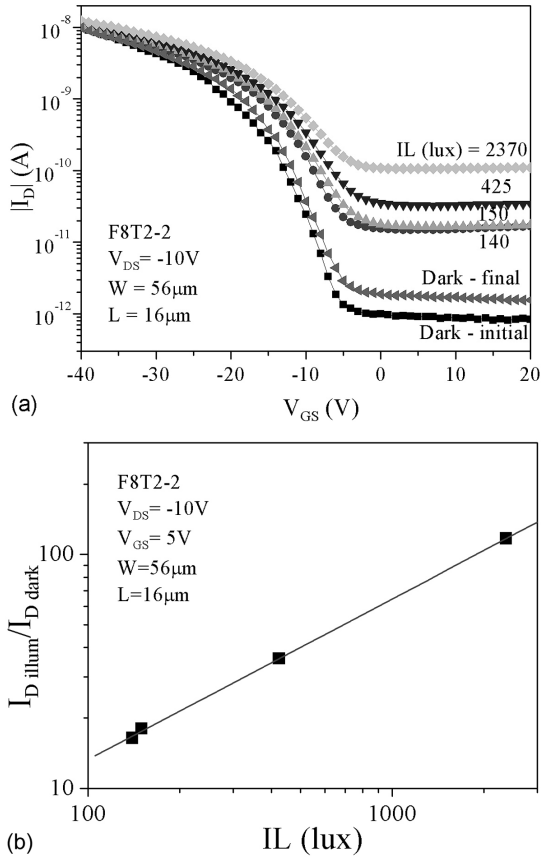

FIGURE 9 — (a) Typical OP-TFT transfer characteristics in the dark and under white illumination. (b) Ratio of drain current under illumination to drain current in the dark as a function of the illuminance.

We should note that these experiments involve dc voltage and are therefore not representative of the real TFT operation during the addressing of an active-matrix display. In AMPLEDs, the driving scheme forces a dc drain current stress on the driving TFT, while in AMLCDs the driving scheme results in an ac gate voltage stress. Both cases require specific OP-TFT characterizations that need to be done using dedicated driving schemes before any definitive conclusion can be drawn regarding the OP-TFT instabilities during typical active-matrix display addressing.

Although the OP-TFT ON-current requirements are the most critical for many active-matrix arrays, the OFF current also needs to be low. The OP-TFT OFF-current can be quite large under certain operating conditions and is not yet fully understood, which makes its optimization difficult. We have recently shown[34] that OP-TFTs are usually very photosensitive, as shown in Fig. 9(a). The OFF-current increase is directly correlated to the illumination level, as shown in Fig. 9(b) and can reach two decades for a white-light illumination of 2370 lux. The ratio of drain current under illumination to drain current in the dark exhibits a power-law dependence with the illuminance, with an exponent of 0.7, which could be associated with the presence of traps in the organic semiconductor. This OP-TFT photosensitivity could result in significant leakage current in AMLCDs due to the high backlight intensity. Increasing the gate/source-drain overlap to reduce this effect is usually not desired because it would increase the parasitic capacitances. Consequently, we believe that, even with a bottom-gate TFT structure, an additional light shield may be needed.

Another issue concerns the fabrication of organic-polymer-based devices, which needs to be compatible with the remaining fabrication process of the FPD. Test structures in which almost no patterning of organic and inorganic layers is involved are the most widely used devices, so far, in many laboratories, but cannot be used in realistic applications. The devices presented here do include a defined gate electrode and planarization technology as shown in Fig. 1, but the organic semiconductor was not defined. A polymer patterning method providing small feature sizes and allowing alignment of successive levels is essential if we want to fabricate high-performance organic polymer devices for all-organic FPDs. Finally, most organic semiconductors are very sensitive to oxygen and moisture and their performance can degrade rapidly when exposed to air. Packaging is therefore critical and would need to be included in the FPD fabrication process. The interaction of the organic semiconductor with the liquid crystal should also be considered.

4 Conclusion

We have presented OP-TFTs based on a spin-coated organic polymer with field-effect mobility values around $5{\cdot}10^{-3}$ cm^2/V-sec, ON-OFF current ratio up to 10^5, and subthreshold slope down to 1.5 V/dec. A detailed analysis of the electrical performance of the devices was presented, including a characterization of the OP-TFT source and drain series resistances and a study of the gate-voltage dependence of the field-effect mobility. Although significant progress has been made over the last decade with regards to OP-TFTs fabrication methods and electrical performances, we believe that today this technology is not fully mature and might not yet be applicable to active-matrix arrays for commercial FPDs. However, the OP-TFTs could soon be used in less-demanding applications requiring displays with lower resolution.

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