

SUPPORTING INFORMATION

Graphene Ambipolar Nanoelectronics for High Noise Rejection Amplification

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S1. Materials and Device Fabrication

A pristine single layer graphene film is first synthesized by chemical vapor deposition (CVD) method on copper foil. One side of the copper sample is coated with 950 PMMA A2 (MicroChem) photoresist as protection layer and the other side is exposed to oxygen plasma to etch away the undesired graphene. The sample is left in ammonium persulfate solution (0.023 g/ml) to dissolve away the copper layer underneath, and then the graphene film with PMMA coating is cleaned and transferred onto prepared intrinsic silicon wafer with 300nm thermal SiO₂ on top. After removing the PMMA coating by rinsing with acetone and isopropyl alcohol, the single layer graphene is then patterned into the desired shape (W/L = 50μm/20μm) by conventional photolithography and oxygen plasma etching. After graphene patterning, Cr/Au (5nm/50nm) source and drain metal contacts are deposited by e-beam evaporation and photolithography lift-off processes, leaving 7 μm length and 50 μm width graphene film in between as device channel. Then 2 nm aluminum layer is e-beam evaporated onto the sample, followed by 12 hours oxidation in air and additional 13.5 nm Al₂O₃ deposited by atomic layer deposition (ALD) at 250 °C. The total thickness of Al₂O₃ is 16.1 nm, which is used as our top gate dielectric layer. Finally, two 2 μm wide Cr/Au (5nm/50nm) top gate metal strips with 1 μm spacing are deposited by e-beam evaporation and photolithography lift-off processes.

S2. Carrier Mobility Extraction

The contact resistance and the carrier mobility can be extracted by fitting the experimental value of resistance across the source and drain of the graphene transistor with the following equation,

$$R_{total} = \frac{V_{ds}}{I_{ds}} = R_{contact} + \frac{L}{q\mu W \cdot \sqrt{n_0^2 + \left(\frac{C_{ox}(V_g - V_{Dirac})}{q}\right)^2}}$$

where the variables are defined as drain-to-source voltage V_{ds} , drain-to-source current I_{ds} , contact resistance $R_{contact}$, channel length L and width W , mobility μ , residual carrier concentration n_0 , gate capacitance C_{ox} , the gate bias voltage V_g , and the charge neutrality point V_{Dirac} . The fitting of data in Figure 1c yield a hole mobility of $844 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and electron mobility of $866 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ with n_0 of $1.57 \times 10^{12} \text{ cm}^{-2}$ and $R_{contact}$ of 378Ω .

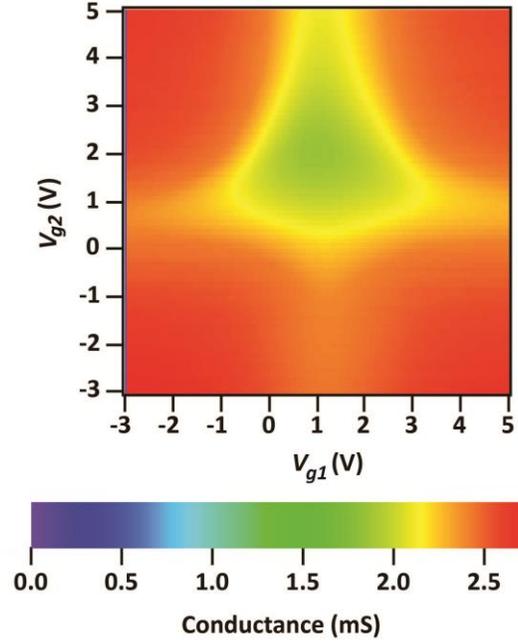


Figure S1. The two-dimensional color plot of conductance versus gate biasing voltages for dual-gate graphene ambipolar device. The graphene channel can be operated under p-p (lower left), n-n (upper right), p-n (upper left), and n-p (lower right) regions by biasing two gate accordingly.

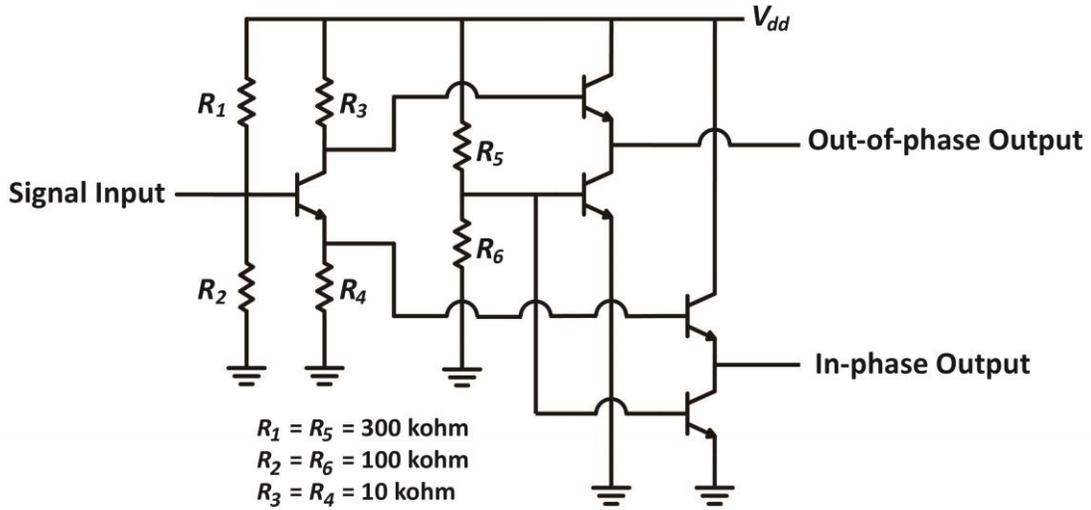


Figure S2. The circuit diagram of the home-built phase shift module with 2N3904 NPN BJTs.

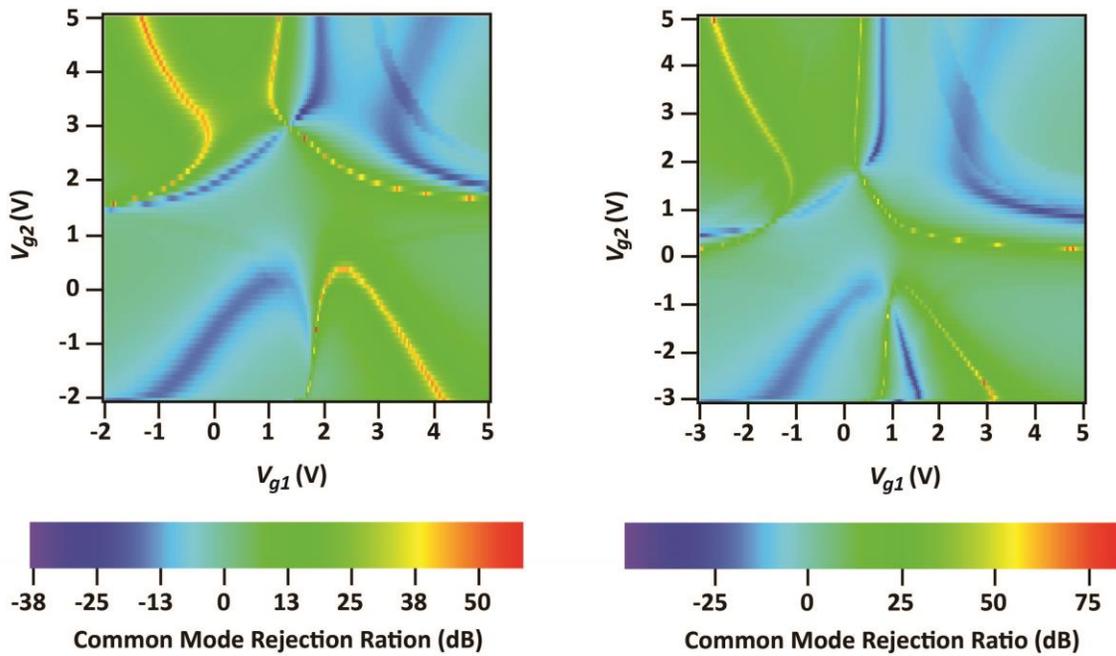


Figure S3. The two-dimensional color plot of CMRR versus dual-gate biasing voltages for two other devices. Measurements are done under the same condition as in Figure 4, and high noise rejection is once again confirmed.

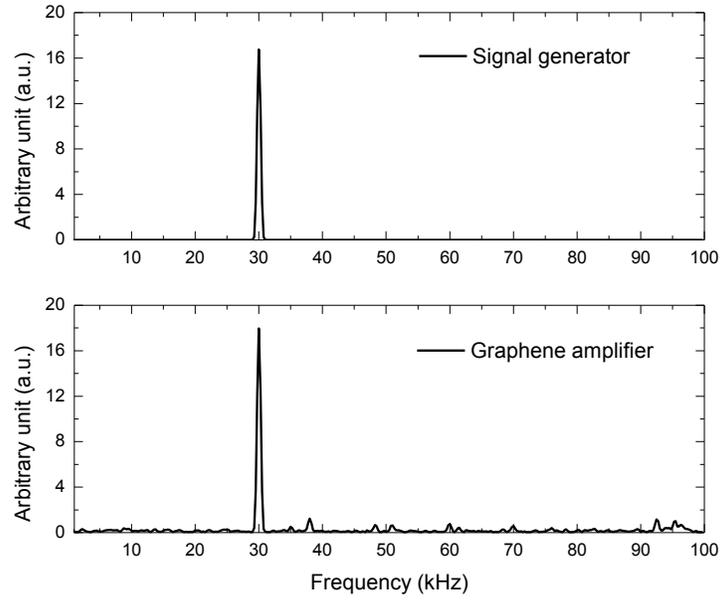


Figure S4. Frequency spectrum analysis by using a commercial FFT spectrum analyzer (Stanford Research System SR760). The carrier frequency is 30 kHz. We do notice small peaks at higher frequency, but not at the harmonics of the carrier frequency. These are likely due to the measurement setup and the home made phase shift module.

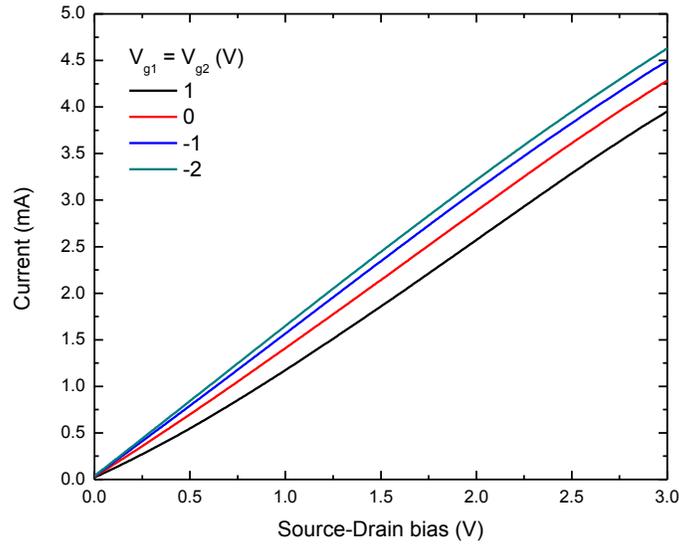


Figure S5. Output characteristics I - V_{ds} of dual-gate graphene amplifier under different gate bias.