Supplementary Information for

Flexible and Transparent All-Graphene Circuits

for Quaternary Digital Modulations
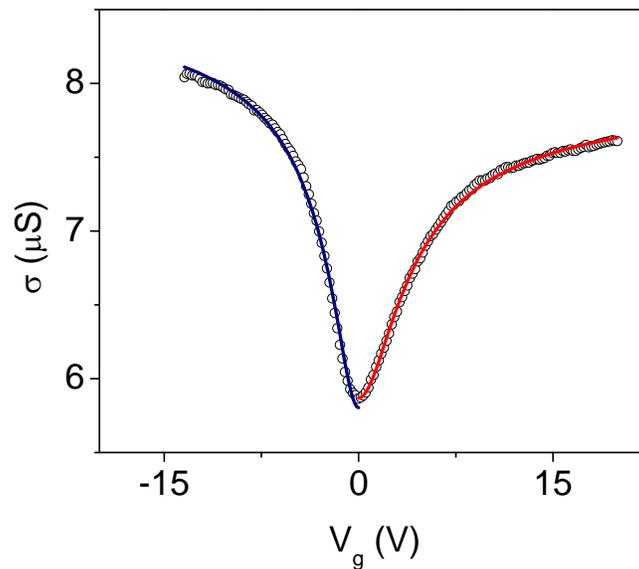
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Supplementary Figures

Supplementary Figure S1, Conductance as a function of gate voltage (round symbols) and its fittings (solid line) for a typical device. The blue and the red solid lines correspond to the fittings for hole and electron mobility respectively. See Methods for details on the fitting method.
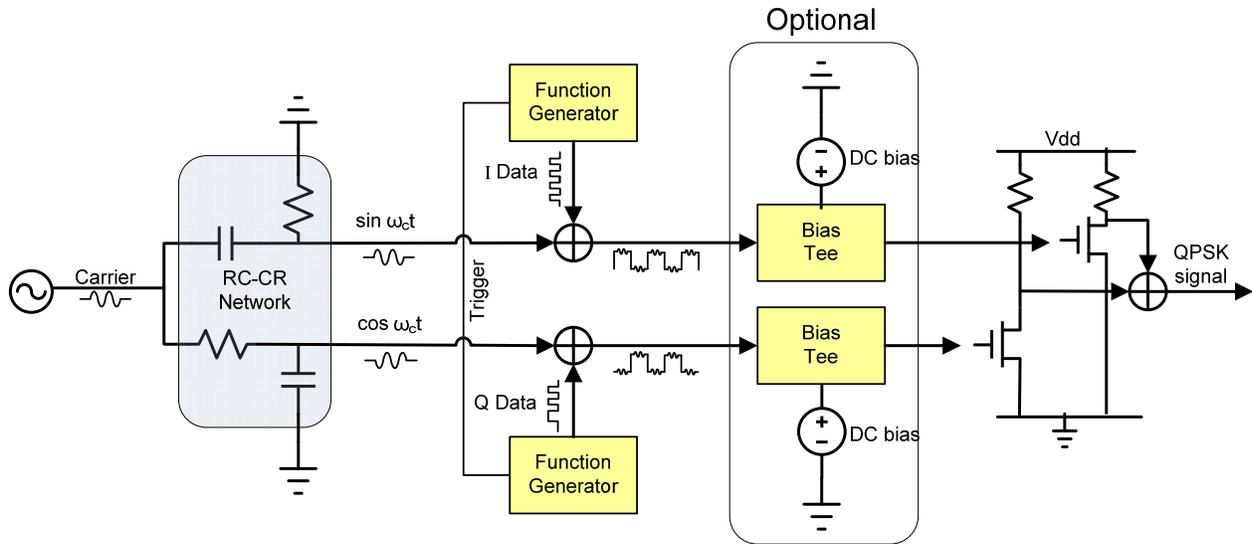
Supplementary Figure S2, Detailed measurement setup for quadrature phase shift-keying signal generation. A sinusoidal carrier signal is generated from a signal generator and fed to an RC-CR phase shift network. The phase of the sinusoidal signal is shifted by +45 and -45 when it passes through RC and CR structure respectively. The resulting two orthogonal functions ($\sin \omega_c t$ and $\cos \omega_c t$) with a phase difference of 90° are summed internally in two different function generators with its respective digital data signal shown as the square wave. The two function generators are phase matched using the trigger function. If the charge neutrality point (V_{Dirac}) is not centered at zero voltage due to environmental doping, the signal can be connected with a bias tee with a DC bias and then fed to the gate of each transistor. When the DC bias is approximately equal to V_{Dirac}, the phase modulation of each transistors will be symmetric. If the Dirac point at 0 voltage, the signals can be directly inserted to the gates of each transistors without a bias tee The two generated signals which are the final quadrature phase-shift keying signals were added internally and measured with an oscilloscope.
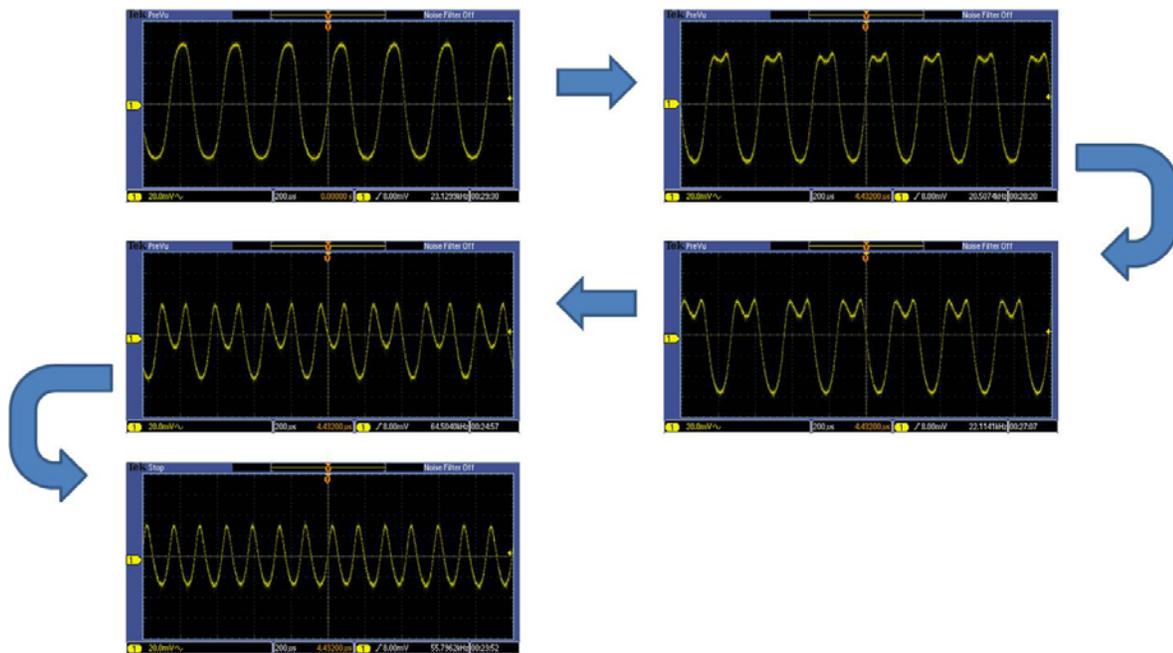
Supplementary Figure S3, Oscillscope images of the frequency doubling as a result of gradual gate bias shift. As the gate DC bias point shifts from the negative side (hole carrier dominated) to the Dirac point, frequency doubling due to ambipolar characteristics of graphene transistor can be observed. If the DC bias point is not exactly at the Dirac point, the output signal will show asymmetry.
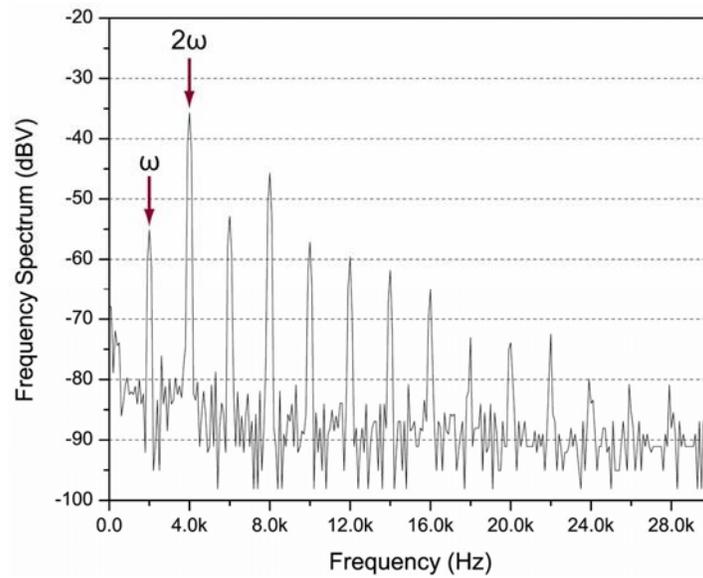
Supplementary Figure S4. Fast Fourier Transform (FFT) of a typical frequency doubled signal. A typical Fast Fourier Transform (FFT) of the doubled signal from a mechanically strained graphene transistor is shown. The radius of curvature was 5.5mm for this plot. The doubled frequency (2ω) term and the original frequency (ω) term has a signal amplitude difference of 20 dBV. The higher order terms also shows significantly weaker signal strength compared to the doubled frequency. The higher order terms can be filtered out if necessary.

Supplementary Table

Publication	Gain	Modulation frequency	Comments
Wang et.al.[25]	0.005	10 kHz	Frequency doubling
Yang et. al.[24]	~0.01	4-10 kHz	BPSK, BFSK
Hsu et. al.[29]	0.005	500 Hz	BPSK
Harada et.al. [28]	~0.05	30 kHz	BPSK
Sordan et.al. [44]	<0.025	100 Hz	Boolean logic
This work : binary modulation	**0.03~0.07.**	**10 kHz**	**BPSK, BFSK, BASK. The first demonstration of BASK.**
This work : quaternary modulation	**4ASK : 0.03 QPSK : 0.06**	**10 kHz**	**4-ASK, QPSK. The first demonstration of quaternary modulations.**

Supplementary Table S1, Signal gain comparison of past works and this work.

Supplementary Reference

44   Sordan, R., Traversi, F. & Russo, V. Logic gates with a single graphene transistor. *Appl. Phys. Lett.* **94**, 073305 (2009).