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# Coulomb blockade in monolayer $MoS_2$ single electron transistor†

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Substantial effort has been dedicated to understand the intrinsic electronic properties of molybdenum disulfide ($MoS_2$). However, electron transport study on monolayer $MoS_2$ has been challenging to date, especially at low temperatures due to large metal/semiconductor junction barriers. Herein, we report the fabrication and characterization of the monolayer $MoS_2$ single-electron transistor. High performance devices are obtained through the use of low work function metal (zinc) contact and a rapid thermal annealing step. Coulomb blockade is observed at low temperatures and is attributed to single-electron tunneling *via* two tunnel junction barriers. The nature of Coulomb blockade is also investigated by temperature-dependent conductance oscillation measurement. Our results hold promise for the study of novel quantum transport phenomena in 2D semiconducting atomic layer crystals.

Atomically thin monolayer and few-layer transition metal dichalcogenides (TMDCs) have garnered much interest recently because of their unique optical and electronic properties. For example, these 2D materials show a transition from an indirect band gap in multilayers to a direct band gap in monolayers,[1,2] which opens up many possibilities in optoelectronics. In addition, the manipulation of valley degrees of freedom was demonstrated by optical pumping through valley-selective circularly polarized light, thus exploiting the valley as information carrier.[3–6] Furthermore, the lack of inversion symmetry in monolayer $MoS_2$ and other TMDC materials leads to a very strong spin–orbit coupling,[7] a condition necessary for realizing spintronic devices. These remarkable features promise a whole new field of rich physics in electron transport of 2D TMDCs such as coupling of spin and valley physics,[8,9] valleytronics,[6] and quantum-spin-hall (QSH) effect-based devices.[8,10,11]

Significant efforts have also been devoted to understand the electron transport in these semiconducting TMDC atomic layers, represented by the monolayer and few-layer molybdenum disulphide ($MoS_2$).[12–17] The earlier reported carrier mobility of monolayer $MoS_2$ devices was in the range of 0.1–1 $cm^2\ V^{-1}\ s^{-1}$ at room temperature.[14] Recent experimental studies have reported much higher carrier mobility in mono- or bilayer-$MoS_2$ field effect transistors (FET), achieved by encapsulating the device with high-$k$ dielectrics (>200 $cm^2\ V^{-1}\ s^{-1}$),[14] and by annealing the device in a vacuum (~1000 $cm^2\ V^{-1}\ s^{-1}$ at 4 K).[18–20] Moreover, the understanding of fundamental electron transport in thin-layered $MoS_2$ is still in its infancy.[21] One of the major hurdles to electron transport study lies in the large metal/semiconductor junction barrier for carrier injection, leading to a contact resistance-dominant charge transport, which limits access to intrinsic transport behavior in $MoS_2$.[12,13,21–23] Although various contact metals on few-layered $MoS_2$ have been studied, including low work function metals (Sc and Ti), as well as high work function metals (Ni, Pt, and Au),[13,14] quantum transport study still remains challenging due to the contact-dominant transport at low temperature. To this end, we report the fabrication of a monolayer $MoS_2$ single electron transistor using a low work function zinc metal contact and a thermal annealing-induced metal migration step. We observe Coulomb blockade phenomena at low temperatures and ascribe this transport behavior to the single electron tunneling through an isolated clean quantum dot. Our observation serves as a stepping stone for advancing our understanding of intrinsic electronic properties of $MoS_2$ and provides new directions for implementing novel quantum electronic devices.

The devices discussed in this study were fabricated on monolayer $MoS_2$ flakes obtained from mechanical exfoliation of bulk $MoS_2$. These flakes were deposited on a degenerate n-doped silicon substrate covered with 280 nm thermally-grown silicon dioxide, which serves as a back-gate. Standard electron beam lithography was employed to pattern the source/drain contact of FET devices on the selected flakes. The contact metals consisting of 5 nm Zn and 25 nm Au were deposited by electron-beam evaporation. Zinc was chosen as the contact metal because the work function of zinc is ~4.28 ± 0.02 eV,[24] which is close to the electron affinity of bulk $MoS_2$ ~4 eV,[13] thereby leading to a very small Schottky barrier at the

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metal/semiconductor junction. A device schematic is shown in Fig. 1a. Our monolayer $MoS_2$ FETs have channel width $W$ = 1 μm with source–drain separation ranging from 100 nm to 300 nm, as shown in the scanning electron microscopy (SEM) image in Fig. 1b. Monolayer $MoS_2$ flakes were identified by color contrast from optical images (Fig. S1†)[14] and also confirmed by AFM height measurement, as shown in Fig. 1c.

We first studied electrical characteristics in our fabricated devices in ambient conditions at room temperature (Fig. 1d, 1e, and S2†). The drain current *versus* source bias characteristics from a typical device shows a Schottky barrier-dominated behavior (Fig. 1d, blue curve) similar to earlier reports in monolayer $MoS_2$ transistors.[14] Even though the curve appears linear, it is mainly attributed to thermally-assisted tunneling current through the atomically thin $MoS_2$ layer and not to the ohmic contact formation.[13] The two-terminal resistance determined from the slope is 818 kΩ. To improve the device performance, we performed thermal annealing of the fabricated

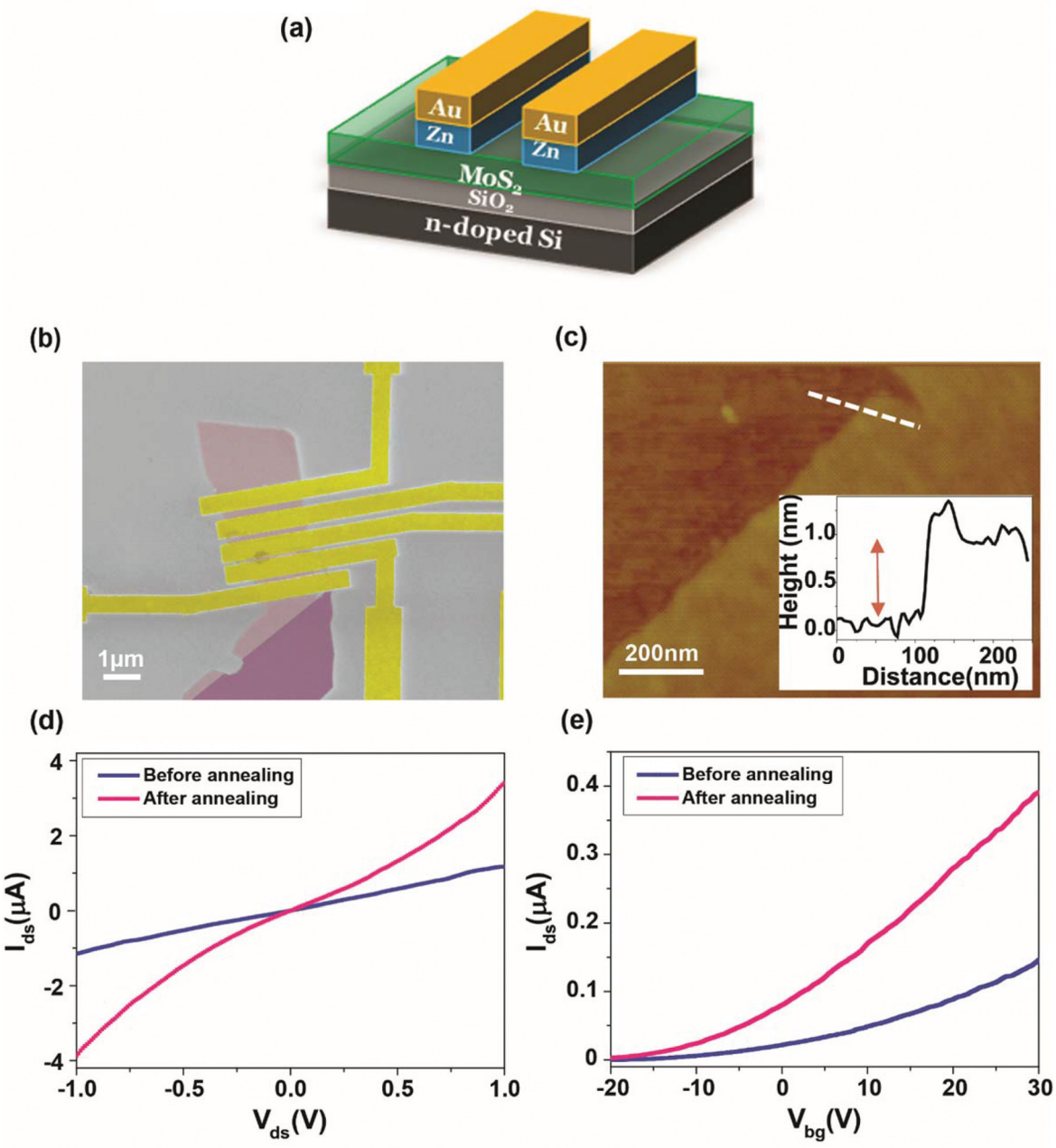


**Fig. 1** Electrical measurements of monolayer $MoS_2$ transistor at room temperature. (a) Schematic of back-gated $MoS_2$ field effect transistor. (b) False colored SEM image of a typical monolayer $MoS_2$ transistor. The lighter pink color represents the monolayer region and electrodes are shown in gold. (c) AFM image of the monolayer $MoS_2$. (Inset) AFM height profile obtained by taking cross-section along the white line on the image. (d) $I_{ds}$–$V_{ds}$ characteristics and (e) transfer characteristics of $MoS_2$ device before (blue) and after (red) rapid thermal annealing for 5 minutes at 250 °C. The applied $V_{ds}$ in (e) is 10 mV.

 

$MoS_2$ transistors in a rapid thermal processing (RTP) furnace under forming gas at 250 °C for 5 minutes. The thermal annealing process has been commonly used to restore a clean surface on channel materials by eliminating oxygen and water adsorbents, leading to substantial enhancement in mobility.[19] As shown in Fig. 1d, the two-terminal resistance drops five-fold to 157 kΩ after annealing. The effect of thermal annealing can also be observed from comparing the transfer curves (Fig. 1d), wherein the transconductance is improved by more than three times and the threshold voltage shifts by about −15 V. The effective mobility for this device was also enhanced by a factor of three after annealing from 8 $cm^2 V^{-1} s^{-1}$ to 26 $cm^2 V^{-1} s^{-1}$. Despite the substantial enhancement, we observed that the slope of $I_{ds}$ *vs.* $V_{ds}$ gets steeper at higher absolute $V_{ds}$ (Fig. 1d), suggesting that the monolayer $MoS_2$ channel is weakly coupled to metallic leads by tunnel barriers.[25] This opaque contact junction provides a suitable platform to study Coulomb blockade phenomena at low temperatures, which has not been possible to date due to lack of control of the metal/$MoS_2$ barrier. We note that increasing the annealing time can further reduce the contact resistance; however, those devices become too transparent for studying single electron tunneling.

Moreover, we investigated the electron transport in our monolayer $MoS_2$ devices at temperatures down to 6 K. Thermal annealing was conducted on the devices prior to the low temperature electrical characterization. The AC conductance of devices was measured with a lock-in amplifier by applying a small AC bias voltage, $v_{ac}$ = 100 μV, superimposed upon a DC bias voltage $V_{ds}$. In Fig. 2a, we plotted the conductance *versus* back-gate voltage ($V_{bg}$) for a representative device with 200 nm channel length with 1 μm width. We observed periodic conductance oscillations as a function of gate voltage ($V_{bg}$). The conductance peaks are separated by suppressed conductance regions with an average peak-to-peak distance of 15 V. This periodic oscillation is associated with single electron charging phenomena, revealing the nature of Coulomb blockade when $k_B T \ll E_C$, where $k_B$ is Boltzmann's constant, $T$ is the temperature, $E_C$ is the dot charging energy. A corresponding two-dimensional conductance map of Coulomb blockade oscillation is plotted as a function of bias voltage ($V_{ds}$) and back-gate voltage ($V_{bg}$) in Fig. 2b. We extract the charging energy from the extent of Coulomb diamond in a bias direction ($V_{ds}$), $E_C$ = 22 meV. This charging energy corresponds to a total capacitance for $MoS_2$ single electron transistor, $C_\Sigma = e^2/E_C$ = 7.27 aF. By calculating the oscillation period along the $V_{bg}$ axis, we estimate a back-gate capacitance, $C_{bg} = e/\Delta V_{bg}$ = 0.0107 aF. Thus, the gate coupling coefficient, $\alpha$ (= $C_{bg}/C_\Sigma$), is determined to be 0.00147. This value allows the conversion of back-gate voltage into a charging energy scale, which is important for a quantitative understanding of transport spectroscopy of our $MoS_2$ device. The unusually small gate coupling coefficient is possibly due to the fringing field screening effect from source/drain electrodes wherein the channel length is much smaller than the thickness of gate dielectric, ~280 nm. Another possibility may be the metal diffusion during the thermal annealing step, which reduces the actual channel length. We also note that

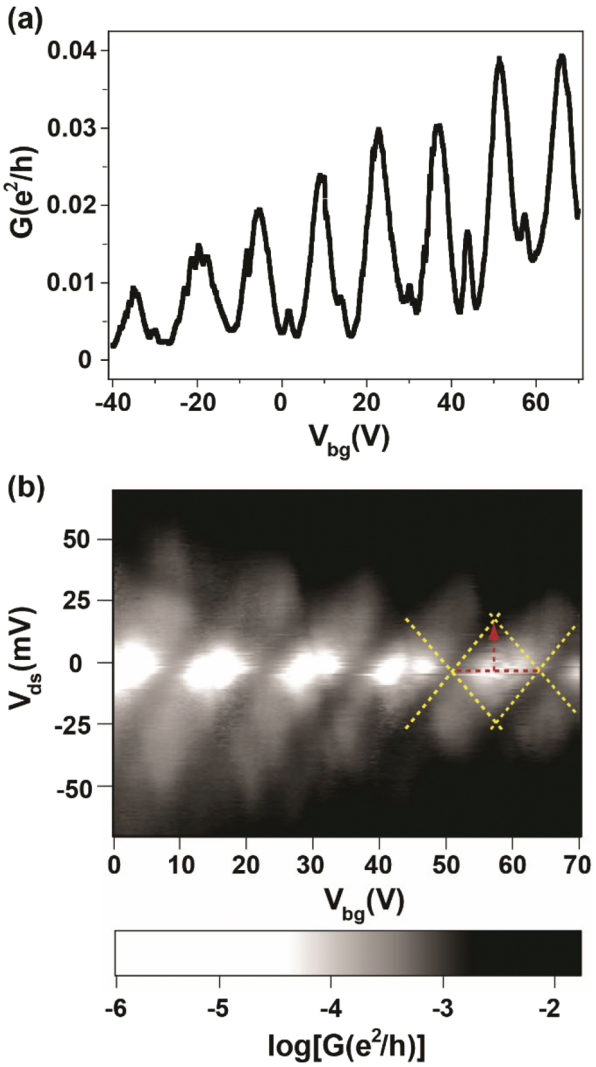


**Fig. 2** Coulomb blockade in monolayer $MoS_2$ SET. (a) AC conductance *G versus* back-gate voltage $V_{bg}$ plot shows clear Coulomb oscillation. $v_{ac}$ = 100 μV. (b) Greyscale plot of conductance *versus* back-gate voltage and bias voltage. The dotted yellow lines provide a visual guide for the Coulomb diamond. The dotted red arrow and red line mark the charging energy ($E_C$) and the gate oscillation period ($\Delta V_{bg}$). All measurements were obtained at 6 K.

there are additional conductance peak lines inside the Coulomb diamonds. This could be due to coupling with a second quantum dot, but the exact origin requires further investigation.

To gain further insight into the effect of contact screening and the origin of the clean Coulomb blockade oscillation, we prepared a back-gated device with 70 nm $Al_2O_3$ as gate dielectric, the thickness of which was chosen for visualizing $MoS_2$ flakes from optical images.[26] The thickness of exfoliated $MoS_2$ flake was also confirmed to be a monolayer by AFM, and the device has a channel length of 100 nm and width of 1 μm. Improvement of the device performance after thermal annealing was once again observed (Fig. S3†).

We now focus on the transport characteristics of the monolayer $MoS_2$ device with $Al_2O_3$ as the gate dielectric at low tem-

perature. The current ($I_{ds}$) *versus* gate voltage ($V_{bg}$) measured at small $V_{dc}$ = 100 μV shows clear conductance oscillations (Fig. 3a). Oscillation peaks in $V_{bg}$ are reasonably periodic and evenly spaced, especially in higher gate voltages wherein the device is heavily n-doped, with a period of $\Delta V_{bg}$ = 0.6 V. In the two-dimensional conductance plot *versus* $V_{ds}$ and $V_{bg}$, the Coulomb diamond features are again present (Fig. 3b), similar to results from devices with 280 nm $SiO_2$ dielectric. Regular closed diamond patterns correspond to single electron charging on a single quantum dot under the gate biasing condition.[27] We estimate the charging energy to be $E_C \approx 17.6$ meV, which corresponds to a total capacitance, $C_\Sigma$ = 9.37 aF. The gate coupling coefficient is calculated to be, $\alpha$ = 0.0285, with $C_{bg}$ = 0.267 aF. Thus, by adopting high-$k$ $Al_2O_3$ as the gate dielectric material, we observe an improvement in electrostatic coupling to the back-gate by a factor of ~20 times.

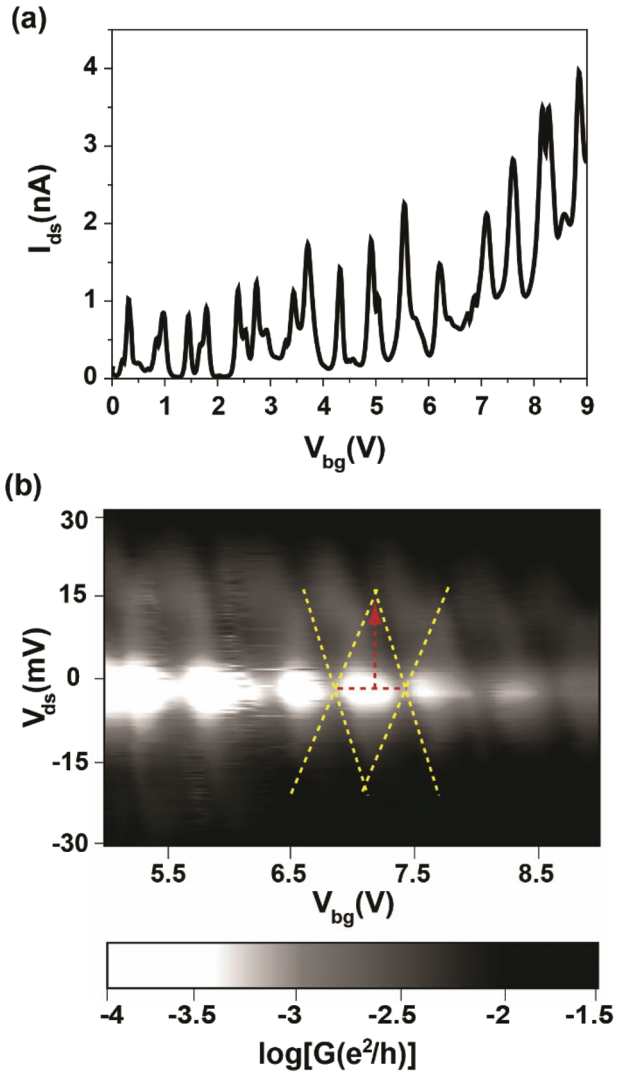


Fig. 3 Coulomb blockade in monolayer $MoS_2$ device with $Al_2O_3$ gate dielectrics. (a) DC conductance *versus* back-gate voltage plot with $V_{ds}$ = 100 μV. (b) Greyscale plot of conductance *versus* back-gate voltage and bias voltage. The dotted yellow lines provide a visual guide for the Coulomb diamond. The dotted red arrow and red line mark the charging energy ($E_C$) and the gate oscillation period ($\Delta V_{bg}$). All measurements were obtained at 6 K.

We also used a commercial finite element analysis simulation tool (COMSOL) to investigate the fringing field screening effect. The displacement field distribution around the $MoS_2$ channel and electrodes was calculated for the device with $SiO_2$ and $Al_2O_3$ as the gate dielectric layers, respectively (Fig. S4†). The resulting low field intensity (dark blue colored area) around the centered part of the $MoS_2$ channel indicates that most of the back-gated area does not contribute to gate capacitance due to screening by electrodes. This screening effect was more pronounced on the device with 280 nm $SiO_2$ as a dielectric layer than on that with 70 nm $Al_2O_3$ as a dielectric layer. Given the dielectric constants of $SiO_2$ ($\varepsilon_{SiO_2}$ = 3.9) and $Al_2O_3$ ($\varepsilon_{Al_2O_3}$ = 7.8) and the geometry of the studied devices, we estimate the back-gate capacitance ratio ($C_{bg,Al_2O_3}/C_{bg,SiO_2}$) to be around 4 if there is no screening effect. However, we found an electrostatic coupling ratio, $\alpha_{Al_2O_3}/\alpha_{SiO_2}$ = 20, and back-gate capacitance ratio = 25. These larger-than-expected values suggest a more significant screening effect in the $SiO_2$ device and the fringing field screening leads to effectively small quantum dot formation.[28] We summarize the parameters of the studied $MoS_2$ SETs in Table 1.

The measured gate capacitance value from Coulomb oscillation is two orders of magnitude smaller than the theoretical gate capacitance of 94.9 aF calculated from the device dimensions. This large difference cannot be explained entirely by the electrode screening effect. We suspect that the metal diffusion is also accounts for the formation of much smaller dots than the device dimension. In fact, we observed that source and drain electrodes were shorted in most of the devices with 50 nm channel length after the thermal annealing process. Note that Coulomb blockade was not present before thermal annealing in all the studied $MoS_2$ SETs. These results indicate that metal diffusion plays a crucial role in the formation of the single electron transistor. In addition, Coulomb blockade was mainly observed in our monolayer $MoS_2$ devices, but rarely

Table 1 The parameters of studied $MoS_2$ devices obtained from Coulomb blockade measurements

| Gate dielectric | Dimension $L \times W$ | $\Delta V_{bg}$ (V) | $\Delta V_{ds}$ (mV) | $C_\Sigma$ (aF) | $C_{bg}$ (aF) | $\alpha$ | Effective area (nm$^2$) |
|---|---|---|---|---|---|---|---|
| $SiO_2$ | 200 nm × 1 μm | 15 | 22 | 7.27 | 0.0107 | 0.00147 | 93 |
| $Al_2O_3$ | 100 nm × 1 μm | 0.6 | 17.6 | 9.37 | 0.267 | 0.0285 | 282 |

Effective quantum dot areas are much smaller than the device physical dimension due to fringing field effects and metal migration.

 

observed in multilayer $MoS_2$ devices (~5 layers) (Fig. S5†). This is attributed to the fact that few-layer (>3 layers) $MoS_2$ FETs generally showed much higher conductance compared to monolayer $MoS_2$ FETs,[29] and the contact junction becomes too transparent for single electron charging.

Finally, we investigated the temperature dependence of conductance oscillations as a function of gate voltage, as shown in Fig. 4a. The Coulomb oscillating feature remains discernible even at $T$ = 30 K. We further analyze the conductance peak linewidths (full-width-at-half-maximum, FWHM) at temperatures ranging from 6 K to 30 K (Fig. 4b). The actual electron temperatures, $T_e$, can be extracted from fitting the line shape of the oscillation peaks (see ESI†). We obtained electron temperatures of 11.65 K, 14.44 K, 23.89 K, and 39.5 K for substrate temperatures of 6 K, 10 K, 20 K, and 30 K, respectively. Furthermore, the gate coupling coefficient can be obtained by fitting the temperature dependent peak width.[27] For Coulomb blockade in the classical regime, $\Delta E < k_BT < E_C$, where $\Delta E$ is the single particle level spacing, the relation is described as $\alpha W = 3.52k_BT/e$.[27,30] For Coulomb blockade in the quantum regime, $k_BT < \Delta E$, the relation is given by $\alpha W = 4.35k_BT/e$.[27,30] The electron temperature-dependent peak width is shown in Fig. 4c and the linear temperature dependence agrees with the relation for a classical regime. We further extract the gate coupling coefficient from the fitting to be 0.0293, which is in good agreement with the value obtained directly from the Coulomb diamond plot in Fig. 3b. These experimental results further support our interpretation that electron transport occurs by tunneling through an isolated single quantum dot in a classical regime, which can be described by the so-called orthodox Coulomb blockade theory.[31,32]

We have demonstrated a high quality monolayer $MoS_2$ single electron transistor device that may pave the way for investigating novel quantum transport behaviors in atomically thin-layered TMDCs. We observed Coulomb blockade in monolayer $MoS_2$ FETs at low temperature by selecting the low work

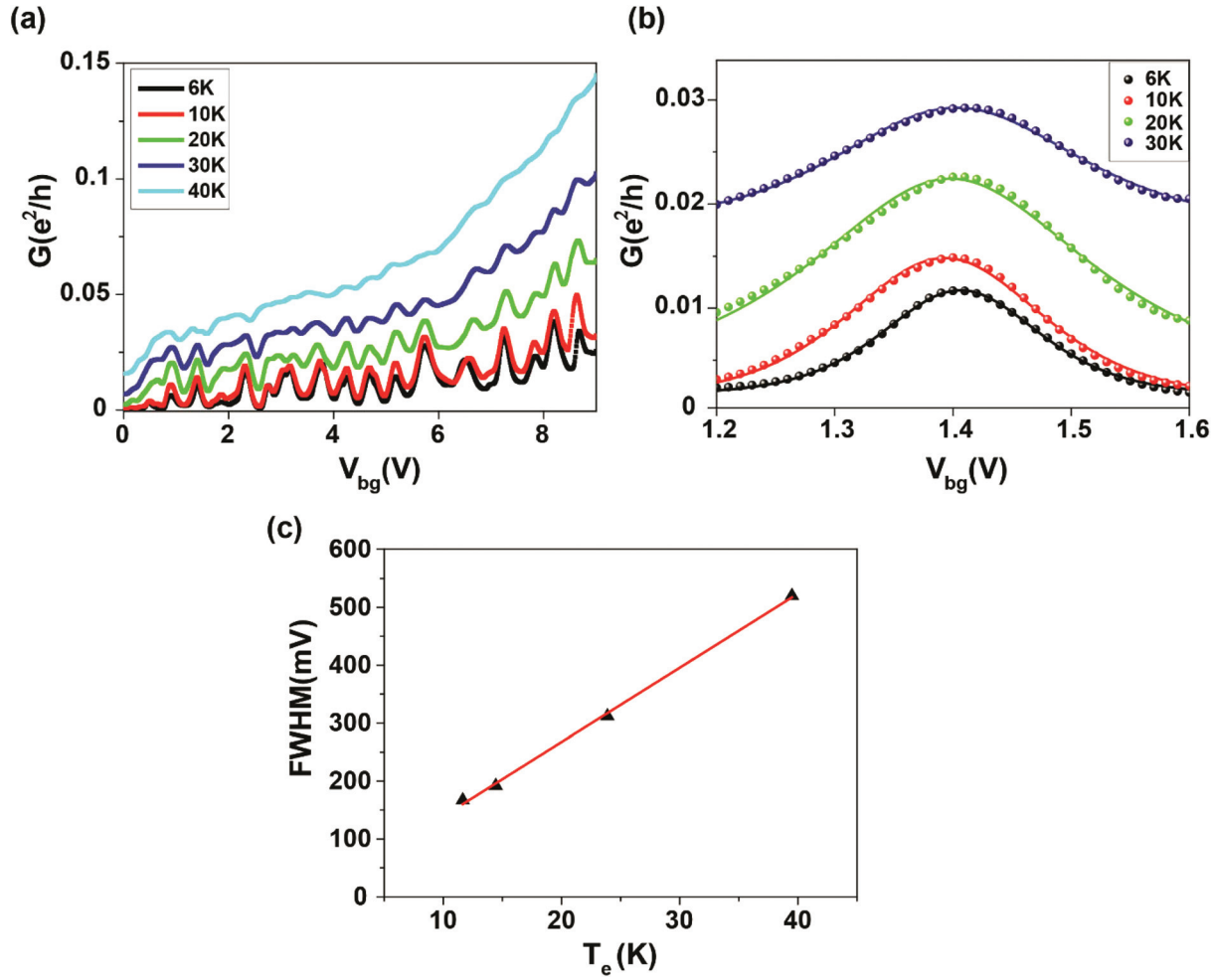


**Fig. 4** Temperature-dependent conductance oscillations. (a) Conductance *versus* back-gate voltage curves measured at different temperatures: $T$ = 6 K (black), $T$ = 10 K (red), $T$ = 20 K (green), $T$ = 30 K (dark blue), and $T$ = 40 K (cyan). (b) Temperature dependence of Coulomb oscillation peaks (color dots). The solid lines are the fits to the experimental data. (c) Full-width-half-maximum (FWHM) values for the Coulomb oscillation peak as a function of electron temperature ($T_e$). The gate coupling coefficient, $\alpha$, is determined to be 0.0293 from the slope of the plot by $\alpha W = 3.52k_BT/e$ for Coulomb blockade in the classical region.

function metal, zinc, as source/drain metal contact, coupled with rapid thermal annealing treatment. Recently, electronic quantum dots formed with TMDCs have been proposed as a suitable platform for realizing quantum bits (qubits) systems due to strong intrinsic spin–orbit splitting states and inversion symmetry breaking.[8,9] Encapsulating $MoS_2$ in a high-$k$ dielectric[14] or in h-BN[20] could improve device quality for further transport study. Our initial results of quantum transport in atomically thin layered $MoS_2$ could serve as a stepping stone for investigating novel quantum effects such as spin-valley coupling and the manipulation of qubit systems.

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